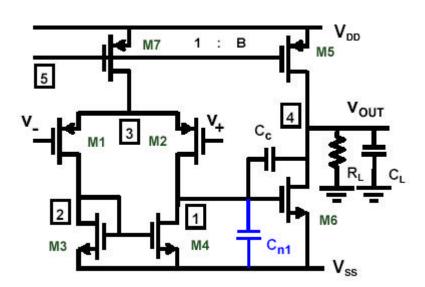
Miller Opamp Design

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This sheet is used to design a low speed Miller Operational Amplifier, using the technique explained by Willy Sansen in his book "Analog Design Essentials" chapters 1 and 6, main slide 0629.

PMOS input devices are chosen as these normally have better matching and lower noise. There is a good explanation of why this is generally better in Analog integrated Circuit Design, Johns, Martin, page 232 Cc in the following schematic is replaced with Cc and Rc in series.

Design Inputs yellow; BSIM inputs blue; outputs green

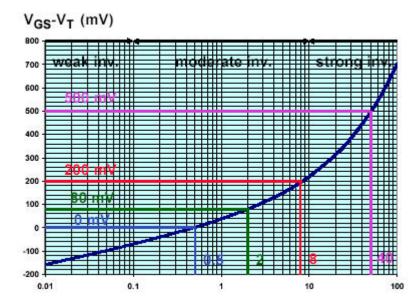


$$kohm := 1000 \cdot ohm \qquad \text{wm} := \frac{m}{10^6}$$

$$q := 1.60217733 \cdot 10^{-19} \cdot \text{coul}$$

$$k_b := 1.380658 \cdot 10^{-23} \cdot \frac{\text{joule}}{K}$$

$$\mathbf{e}_{\text{ox}} := 8.8542 \cdot 10^{-12} \cdot 3.9 \cdot \frac{F}{m}$$



The starting point of the analysis focuses on this graph, which shows the EKV model and gives i the inversion coefficient for Vgs-Vt.

The EKV model allows a single equation to be used for both the striong inversion and weak inversion operating zones on the FET.

This model allows Vgs-Vt (Vgt) to be negative and typically vary from -0.2 to 0.5V. It is unusualy positive, otherwise the ROUT is too low and we get no gain.

STEP 1. Design requirements in yellow. Blue are the BSIM3 MOS parameters. CL = a Cc, Cc = B Cgs6, F6 = ? GBWNormally these are 2 3 2

$$TOX := 510^{-9} \text{m}$$

$$U0_n := 388 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}$$

$$UO_n := 388 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}$$
 $UA_n := 6.5 \times 10^{-9} \frac{\text{m}}{\text{V}}$

$$UB_n := 4.2 \times 10^{-18} \cdot \frac{m^2}{v^2}$$

$$NFACTOR_n := 1.14$$

$$VTHO_n := 0.633V$$

$$VSAT_n := 86301 \frac{m}{s}$$

$$U0_p := 139 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}$$

$$UA_p := 1.399 \times 10^{-9} \frac{m}{V}$$

$$U0_{p} := 139 \frac{cm^{2}}{V \cdot s} \qquad UA_{p} := 1.399 \times 10^{-9} \frac{m}{V} \qquad UB_{p} := 1.0 \times 10^{-19} \cdot \frac{m^{2}}{V^{2}}$$

 $NFACTOR_p := 1.54$

 $VTH0_p := 0.673V$

 $VSAT_p := 103503 \frac{m}{s}$

STEP 2. From U0 and the other BSIM mobility parameters, calculate the mobility for the NMOS and the PMOS devices as this changes with Vgt. The equations for this are from W Liu "Mosfet Models for Spice Simulation", page 249. Assume MOBMOD=1 which is the default.

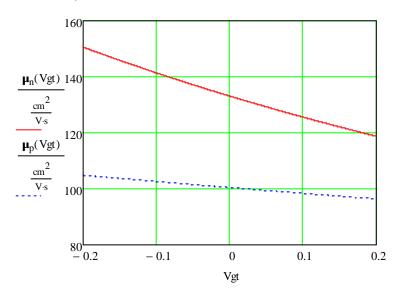
$$\begin{split} \pmb{\mu}_n(Vgt) \coloneqq \frac{U0_n}{1 + UA_n \cdot \frac{Vgt + 2 \cdot VTH0_n}{TOX} + UB_n \cdot \left(\frac{Vgt + 2 \cdot VTH0_n}{TOX}\right)^2} \end{split}$$

$$\begin{split} \pmb{\mu}_p(Vgt) \coloneqq \frac{U0_p}{1 + UA_p \cdot \frac{Vgt + 2 \cdot VTH0_p}{TOX} + UB_p \cdot \left(\frac{Vgt + 2 \cdot VTH0_p}{TOX}\right)^2} \end{split}$$

$$\mu_{n}(Vgt6) = 118.769 \cdot \frac{cm^2}{V \cdot s}$$

This shows how the mobility changes with Vgt for both the NMOS and PMOS

It is 50% higher for the NMOS



STEP 3. Calculate FT (frequency at which gain equals 1) for transistor M6 to get the gain-bandwidth. From this we can calculate L (Gate Length) and we use this same L for most of the transistors. The EKV model is used here, as this is what Samson uses, refer slides: 0138, 0140, 0165, 0627. The gate length needs to be at least twice the minimum.

$$V_{GSTtn} := 2 \cdot NFACTOR_n \cdot \frac{k_b \cdot T}{q}$$
 0138

$$i(Vgt) := \left[\ln \left[e^{\left(\frac{Vgt}{V_{GSTtn}} \right)} + 1 \right]^{2} \right]$$
 0138

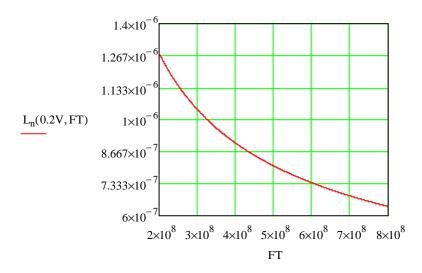
$$GM(Vgt) := \frac{1 - e^{-\sqrt{i(Vgt)}}}{\sqrt{i(Vgt)}} \quad \textbf{0140}$$

$$F_{T} := \mathbf{a} \cdot \mathbf{\beta} \cdot ? \cdot \left(1 + \frac{1}{\mathbf{\beta}}\right) \cdot GBW \quad \mathbf{0627}$$

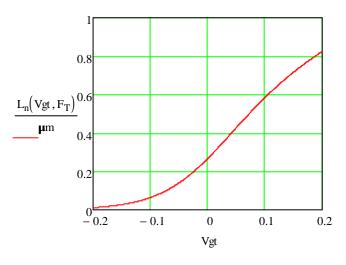
$$L_n\!\!\left(Vgt,F_T\right) \coloneqq \sqrt{\frac{\boldsymbol{\mu}_n(Vgt)\!\cdot\!\frac{k_b\!\cdot\!T}{q}}{\boldsymbol{p}\!\cdot\!F_T}\!\cdot\!\!\left[\!\sqrt{i(Vgt)}\!\cdot\!\!\left(1-e^{-\sqrt{i(Vgt)}}\right)\right]} \quad \boldsymbol{0165}$$

$$V_{GSTtn} = 0.053 \cdot V$$
 $i(Vgt6) = 14.386$

$$L_n(Vgt6, F_T) = 0.824 \cdot \mu m$$
 $F_T = 480 \cdot MHz$



This graph shows how the length of the gate influences the FT (the frequency at which the gain is 1)



We also get this strange graph that shows how the required gate length changes with Vgt.

STEP 4. Use the following equations to calculate the widths and currents of M6 and M5, which are dependent on CL.

$$C_c \coloneqq \frac{C_L}{\boldsymbol{a}} \qquad C_{gs6} \coloneqq \frac{C_L}{\boldsymbol{a} \cdot \boldsymbol{b}} \qquad \textbf{0621} \qquad \qquad C_{ox} \coloneqq \frac{\boldsymbol{e}_{ox}}{TOX} \qquad \qquad W_6 \coloneqq C_{gs6} \cdot \frac{3}{2} \cdot \frac{1}{L_n(Vgt6, F_T) \cdot C_{ox}} \qquad \textbf{016}$$

$$I_{DSt6} \coloneqq \pmb{\mu}_n(Vgt6) \cdot C_{ox} \cdot \frac{W_6}{L_n(Vgt6, F_T)} \cdot \left(V_{GSTtn}\right)^2 \\ I_{DS6} \coloneqq I_{DSt6} \cdot \left(\ln\left(1 + e^{\ln\left(e^{\sqrt{i(Vgt6)}} - 1\right)}\right)\right) \\ \pmb{0138}$$

$$g_{m6} \coloneqq \frac{GM(Vgt6) \cdot I_{DS6} \cdot 2}{V_{GSTtn}} \qquad \textbf{0141} \\ g_{m6} = 0.302 \cdot \frac{mA}{V} \\ I_{DS6} = 31.099 \cdot \mu A \qquad \qquad V_{6} = 29.278 \cdot \mu m$$

STEP 5. We need the Early voltage for M6 so that we can calculate the output resistance to get the voltage gain. From this we can convert Cc to the equivalent input capacitance from the Miller equation. **W Liu "Mosfet Models for Spice Simulation"**, **equations A-62**, **A-78**. The equivalent Early voltage is VA and this converts to the ro6 by the slope at the point of operation. The output impedance is halved as M5 needs to be considered and is assumed to be equal to rout of M6. Also a 1/2 adjustment is made for ro, as we are working near VTH0 and ro is reduced.

$$\mathbf{e}_{\text{sat6}} \coloneqq \frac{2 \cdot \text{VSAT}_{\text{n}}}{\mathbf{\mu}_{\text{n}}(\text{Vgt6})} \qquad \text{VA6} \coloneqq \mathbf{e}_{\text{sat6}} \cdot \text{L}_{\text{n}}\big(\text{Vgt6}, \text{F}_{\text{T}}\big) \qquad \text{ro6} \coloneqq \frac{1}{2} \left(\frac{\text{VA6} + \text{VTH0}_{\text{n}} + \text{Vgt6}}{\text{I}_{\text{DS6}}}\right) \qquad \text{ro5} \coloneqq \text{ro6}$$

$$Vgain6 := g_{m6} \cdot \frac{ro6}{2}$$

$$V_{gain6} := g_{m6} \cdot \frac{ro6}{2}$$

$$C_{n1} := C_{gs6} + (1 + V_{gain6}) \cdot C_{c}$$

$$ro6 = 2.06 \times 10^5 \cdot ohm$$

 $VA6 = 11.979 \cdot V$

$$Vgain6_dB := 10 \cdot log(Vgain6)$$

$$C_{n1} = 10.818 \cdot pF$$

Vgain6 = 31.119

Vgain6 dB = 14.93

STEP 6. Now scale M1 and M2. Keep Vgt1 low to minimise noise. B needs to be high to save current, but recommend this is kept at 1. L needs to be greater than twice the process minimum.

$$g_{m1} := 2 \cdot \mathbf{p} \cdot C_{n1} \cdot GBW$$
 063

$$I_{DS1} := \frac{I_{DS6}}{2 \cdot B}$$

$$I_{DS1} := \frac{I_{DS6}}{2 \cdot B} \qquad \qquad GM1 := \frac{g_{m1}}{I_{DS1}} \cdot NFACTOR_p \cdot \frac{k_b \cdot T}{q} \qquad \textbf{014}$$

Given
$$GM1 = \frac{1 - e^{-\sqrt{i}}}{\sqrt{i}}$$
 $i := Find(GM1)$

$$V_{GSTtp} \coloneqq 2 \cdot NFACTOR_p \cdot \frac{k_b \cdot T}{q}$$

$$L_p := \sqrt{\frac{ \boldsymbol{\mu}_p(Vgt1) \cdot \frac{k_b \cdot T}{q}}{\boldsymbol{p} \cdot \frac{F_T}{4}} \cdot \left[\sqrt{i} \cdot \left(1 - e^{-\sqrt{i}} \right) \right]} \quad \begin{array}{l} \textbf{0165} \\ \textbf{and 065 for FT} \end{array}$$

$$W_1 := \frac{\frac{I_{DS1}}{i} \cdot L_p}{\mu_p(Vgt1) \cdot C_{ox} \cdot \left[\left(V_{GSTtp} \right)^2 \right]}$$
 0138

$$W_4 := \frac{W_6}{2} \cdot \frac{1}{B}$$

$$W_4 := \frac{W_6}{2} \cdot \frac{1}{B}$$
 $g_{m1} = 1.359 \cdot \frac{mA}{V}$ $U_1 = 36.276 \cdot \mu$

STEP 7. Calculate the voltage gain for stage 1 and then calculate the overall voltage gain. The output resistance is the Early voltage divided by the current. This is halved because both there are two FETS and the gain is halved again as we are working near VTH0 and the output resistance is slightly lower at this point.

$$\boldsymbol{e}_{sat1} \coloneqq \frac{2 \cdot VSAT_p}{\boldsymbol{\mu}_p(Vgt1)} \qquad \qquad VA1 \coloneqq \boldsymbol{e}_{sat1} \cdot \boldsymbol{L}_p$$

$$VA1 := \mathbf{e}_{sat1} \cdot L_p$$

$$ro1 := \frac{1}{2} \left(\frac{VA1 + VTHO_p + Vgt1}{\frac{I_{DS1}}{2}} \right)$$

$$Vgain1 := g_{m1} \cdot \frac{ro1}{2}$$

 $Gain_dB := 20 \log(Vgain_1 \cdot Vgain_6)$

 $VA1 = 10.827 \cdot V$

Vgain1 = 507.055

 $Vgain1_dB := 10 \cdot log(Vgain1)$

$$ro1 = 7.46 \times 10^5 \cdot ohm$$

Vgain1 dB = 27.051

STEP 8. Calculate the compensation components Rc and Cc. This is calculated to 5.74, 5.75, 5.76 and according to Analog integrated Circuit Design, Johns, Martin, page 243. The classic method is Rc1, but because we know the output capacitance the Rc3 is a good choice. I have cheated and averaged!!

$$Rc1 := \frac{1}{\alpha}$$

$$Rc1 := \frac{1}{g_{m6}} \qquad Rc2 := \frac{1}{g_{m6}} \left(1 + \frac{C_{gs6} + C_L}{C_c} \right) \qquad Rc3 := \frac{1}{1.2 \cdot g_{m1}} \qquad Rc := \frac{Rc1 + Rc2 + Rc3}{3}$$

$$Rc3 := \frac{1}{1.2 \cdot g_{m1}}$$

$$Rc := \frac{Rc1 + Rc2 + Rc2}{2}$$

 $Rc3 = 0.613 \cdot kohm$

 $Rc1 = 3.31 \cdot kohm$

 $Rc2 = 14.341 \cdot kohm$

Design Requirements

 $C_L \equiv 1pF$ $GBW \equiv 20MHz$ $Vgt6 \equiv 0.2V$ $\mathbf{a} \equiv 3$ $\mathbf{\beta} \equiv 3$? $\equiv 2$

 $B \equiv 1$ $Vgt1 \equiv 0.1V$

Summary of circuit values

$$\begin{split} L_n \big(Vgt6, F_T \big) &= 0.824 \cdot \mu m \\ W_6 &= 29.278 \cdot \mu m \end{split} \qquad \begin{aligned} L_p &= 0.515 \cdot \mu m \\ W_1 &= 36.276 \cdot \mu m \end{aligned} \qquad \begin{aligned} C_c &= 0.333 \cdot pF \\ Rc &= 6.088 \cdot kohm \end{aligned} \qquad \begin{aligned} I_{DS6} &= 31.099 \cdot \mu A \\ Gain_dB &= 83.962 \end{aligned}$$

Ln is the length of all devices except M1 and M2

M1 and M2

W1 is the width of M1 and M2

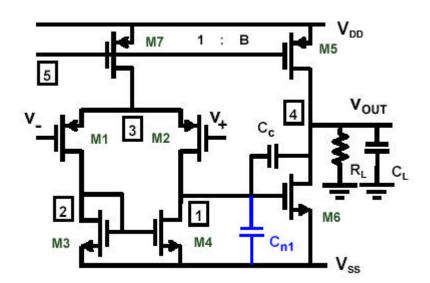
M6, M5 and M7. W4 is the width of M3 and M4

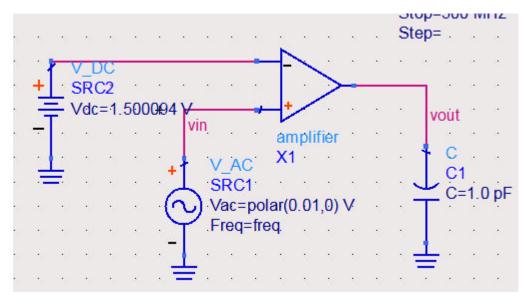
Simulation

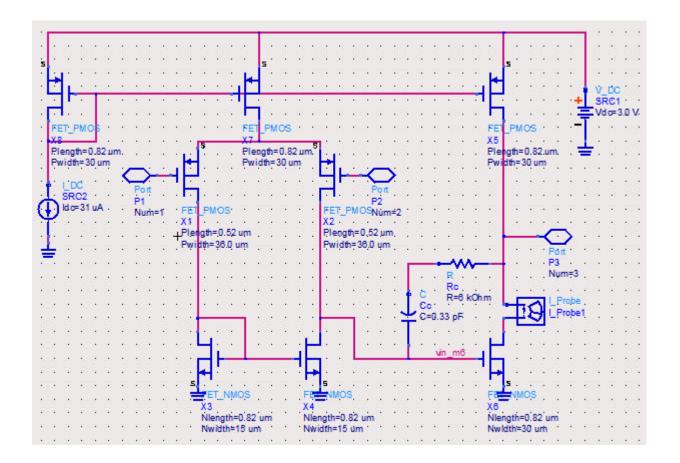
The amplifier is simulated using ADS with BSIM3 parameters available from the BSIM3 website at Berkeley (and used in the calculations). The current reference is set to 31uA which means the **total current excluding the biasing is only 62uA** The output range goes to within 300mV of the rails.

This is a very good amplifier for this current and for such a large output capacitance.

The transistors are not so great







The gain from the first stage is simulated 27.7dB, calculated 27.051dB The gm6 is simulated 0.254mA/V, calculated 0.302mA/V.

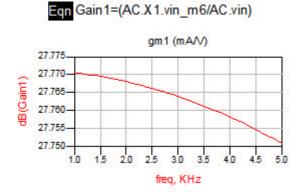
The simulations are better than calculated

$$g_{m6} = 0.302 \cdot \frac{mA}{V}$$

Eqn gm6=(AC.X1.I_Probe1.i/AC.X1.vin_m6)*1000

 $Vgain1_dB = 27.051$

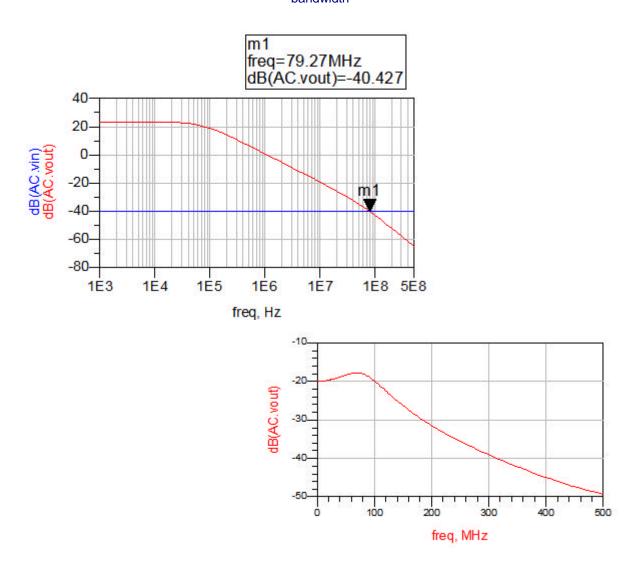




The unity gain frequency is simulated as 80MHz but calculated as 20MHz.

The top sim is open loop and the output signal is compared in amplitute to the input signal in blue

The plot at the bottom is with unity gain showing that there is some peaking and also about 100MHz simulated bandwidth



Rail to rail behaviour of the input in unity gain mode

