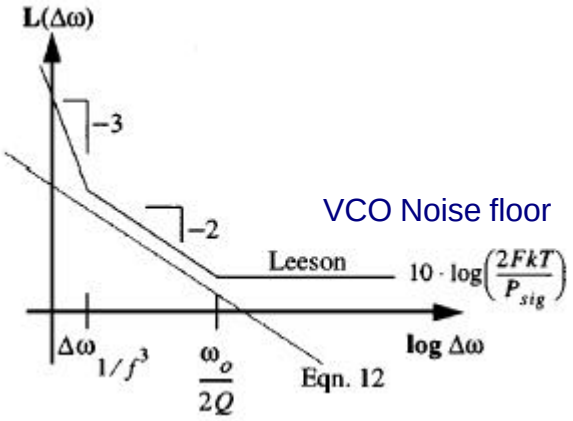
VCO & Synthesiser Design Sheet

This sheet is a general purpose design sheet for LC VCOs and PLLs. The topic is fairly complicated and choices made in the VCO design affect the PLL loop filter settings.

Start by entering the VCO components assuming a Colpitts topology.
Then, calculate the effective VCO Q
Then, calculate the VCO phase noise profile,
Then, the loop bandwidth and the integrated phase noise.

I will try to put some simulation results in soon, but at the moment this looks ok to me.

Chris Haji-Michael
http://www.sunshadow.co.uk/chris.htm



VCO Noise floor

$k_b := 1.388 \cdot 10^{-23} \frac{joule}{K}$ $T := 270 \cdot K$

$fF := 10^{-15} \cdot farad$ $mW := 10^{-3} wat$ $nH := 10^{-9} \cdot henry$

VCO Details, QC is Q for the Capacitor which is assumed to be high compared to the L, The VCO is assumed to be Colpitts.

$f_o := 1.76 \cdot 10^{9} \cdot Hz$

$Q_C := 200$

VCO noise factor F

First calculate the noise factor (F) of the VCO transistor as defined by Rogers & Plett, Radio Freq Integrated Circuit Design (page 286), where **Rp** is the equivalent parallel resistance of the tuned circuit. Note that increasing the oscillator Q increases the noise floor.... not many people know that !!!

The noise equations are from **Gray & Meyer** page 752 and 759
Rb is the transistor bias resistor (Rogers p 271), assume 1V drop at 1mA = 1kohm
Rp is the effective parallel resistor of the VCO tuned circuit
and the higher this is, the higher the VCO **wideband** phase-noise, but the better close in phase noise.

$R_b := 10000 \cdot ohm$

$i_{biasnoise} := \sqrt{\frac{4 \cdot k_b \cdot T \cdot Hz}{R_b}}$

$C(L) := \frac{1}{(2 \cdot \pi \cdot f_o)^2 L}$

$R_C(L) := \frac{Q_C}{2 \cdot \pi \cdot f_o \cdot C(L)}$

$R_L(Q_L, L) := Q_L \cdot L \cdot 2 \cdot \pi \cdot f_o$

$R_p(Q_L, L) := \frac{1}{\frac{1}{R_L(Q_L, L)} + \frac{1}{R_C(L)}}$

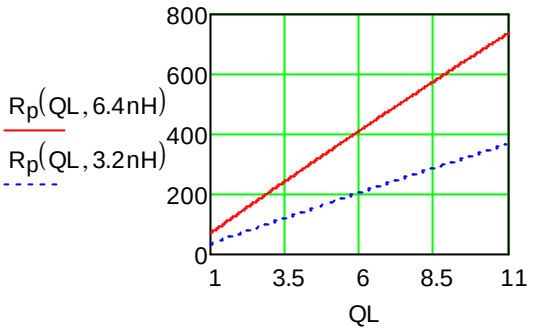
$i_{biasnoise} = 1.224 \times 10^{-12} \cdot amp$

$C(6.4nH) = 1 \times 10^{3} \cdot fF$

$R_p(10, 6.4nH) = 674.036 \times 10^{0}\ \Omega$

$? := 0.5$ $g_m := 50\frac{mA}{volt}$

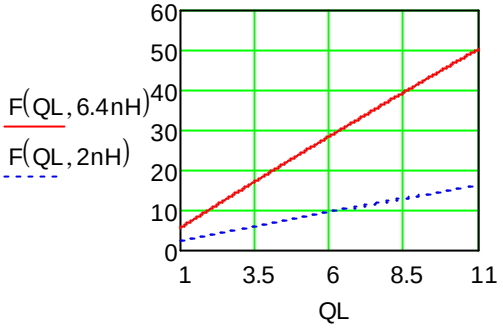
$$i_{transistor} := \sqrt{4 \cdot k_b \cdot T \cdot \frac{2}{3} \cdot g_m \cdot Hz}$$



$$F(Q_L, L) := 1 + \frac{i_{biasnoise}^2 \cdot R_p(Q_L, L) \cdot ?}{k_b \cdot T \cdot Hz} + \frac{i_{transistor}^2 \cdot R_p(Q_L, L) \cdot (1 - ?)}{k_b \cdot T \cdot Hz}$$

$10 \log(F(10, 6.4nH)) = 16.6$

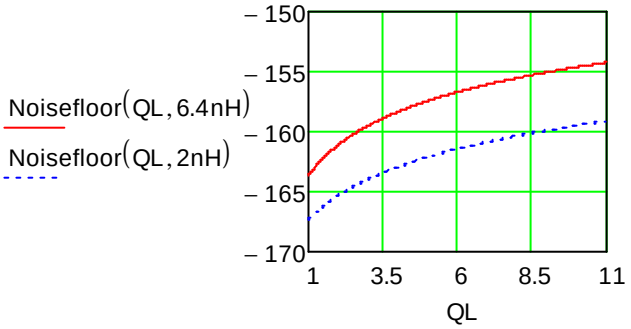
This plot on the right shows the effective noise figure of the VCO under different QL, and inductor values. It also takes into account the bias resistance and the transistor gm, but NOT the transistor noise. The noise figure can be surprisingly high, but this affects the **wideband** phase noise only (noisefloor).



$$Noisefloor(Q_L, L) := 10 \cdot \log\left(2 \cdot T \cdot F(Q_L, L) \cdot k_b \cdot \frac{1}{joule}\right) + 30$$

$Noisefloor(10, 6.4nH) = -154.6$

Noise Floor in dBm



Oscillator Phase Noise

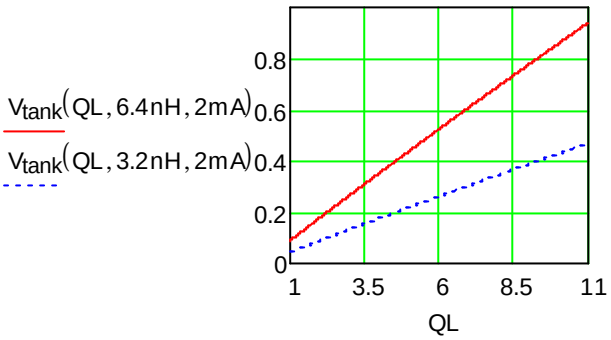
Now that we have the noisefloor, the phase noise can be found from Rogers & Plett, Radio Freq Integrated Circuit Design (page 286), equation 8.90 and adding the affect for noise floor but ignoring flicker noise.

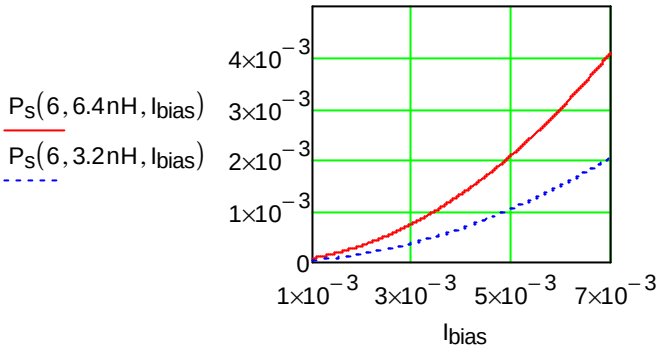
Qt = Q of Oscillator tank
Vtank = peak voltage swing in LC
Ps = power in loop (assumed to be output power)
PN is relative phase noise in dB

$$Q_T(Q_L, L) := R_p(Q_L, L) \cdot \sqrt{\frac{C(L)}{L}}$$ $Q_T(10, 6.4nH) = 9.524$

$$V_{tank}(Q_L, L, I_{bias}) := \frac{2}{\pi} \cdot I_{bias} \cdot R_p(Q_L, L)$$ $V_{tank}(10, 6.4nH, 1.5mA) = 0.64\,V$

$$P_s(Q_L, L, I_{bias}) := \frac{V_{tank}(Q_L, L, I_{bias})^2}{2 \cdot R_p(Q_L, L)}$$ $P_s(10, 6.4nH, 1.5mA) = 0.307 \cdot mW$





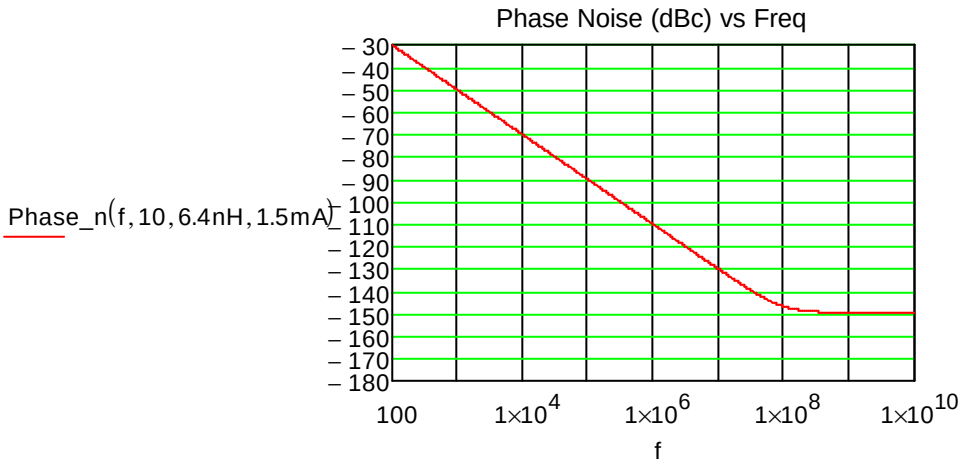
The VCO output power is **assumed to be a quarter** the power in the loop (Ps).

This calculates the phase noise accoding to the Leeson's equation assuming the phase-noise is dominated by the Q, i.e the noise slope is 20dB/decade.
This plot will have the same wideband noise floor as specified above (in dBm)
if Ps (above) is set to 4 * 1mW.

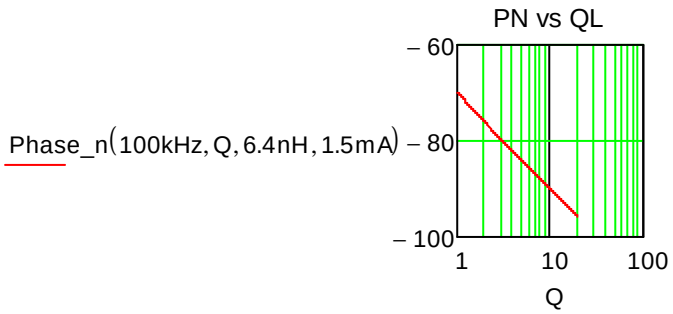
The phase noise is in dBc

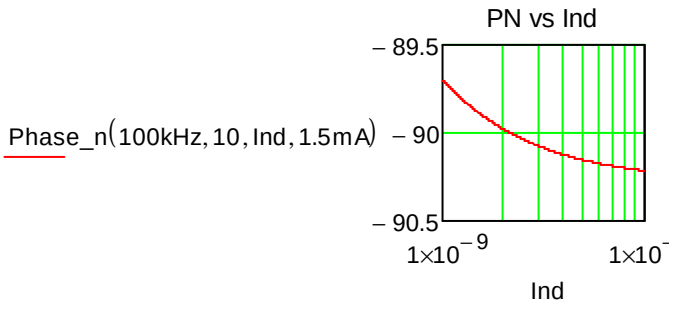
$$\text{Phase\_n}(?\,f, Q_L, L, I_{bias}) := 10\cdot\log\left[\left[1+\left(\frac{f_o}{2\cdot Q_T(Q_L,L)\cdot ?\,f}\right)^2\right]\cdot\frac{2F(Q_L,L)\cdot k_b\cdot T\cdot Hz}{P_s(Q_L,L,I_{bias})}\right]$$

Phase_n(100·kHz, 10, 6.4nH, 1.5mA) = –90.2 Phase_n(500·MHz, 10, 6.4nH, 1.5mA) = –149.3 dBc

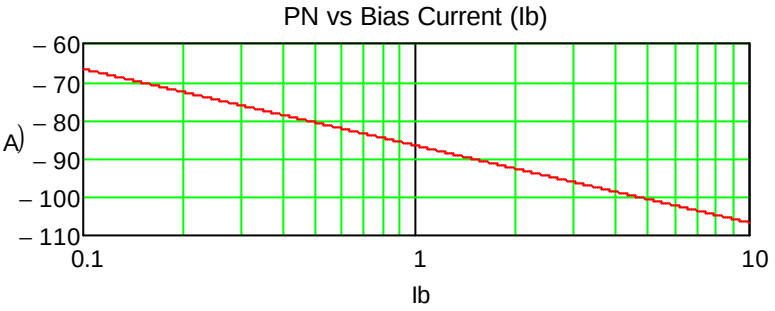


These plots show how the phase noise changes.
There are only two ways to improve the phase noise, increase Q and increase current.

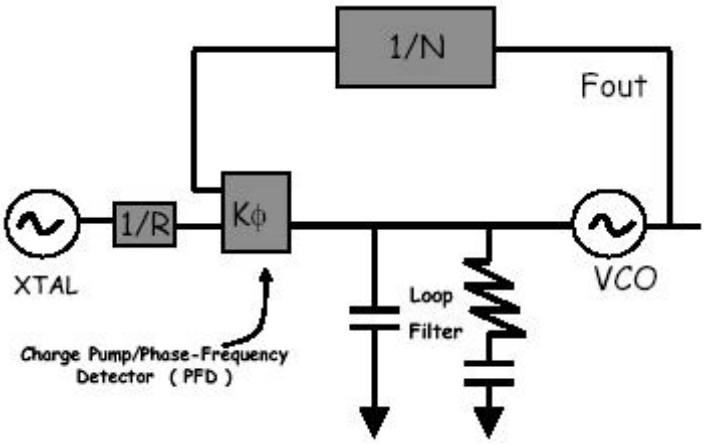




Phase_n(100kHz, 10, 6.4nH, Ibm A)



Next, design the Synth for Minimum Phase Noise...

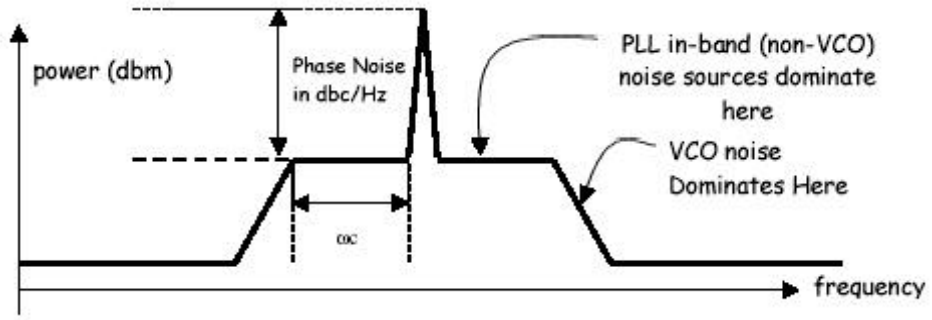


The phase noise calculation inside a synth loop is found from the Deans Book from Nat Semi

The Phase detector phase noise (PDPN) is guessed at and is in dBm/Hz, The limit is typically -207 prf is the phase-reference-freq

$N := 110$ $PDPN := -203$

$prf := \frac{f_o}{N}$ $prf = 16.0 \cdot MHz$



This part calculates the PLL in-band phase-noise in -dBc/Hz. **Fc** is designed to be the point where the VCO noise and the in-loop phase noise are the same as this will minimise the total Phase Noise out of the synth.

First we need to calculate the in-loop phase noise from **PNPD** (phase noise of the phase detector).

$$InLoopPN(PDPN, N) := PDPN + 10 \cdot \log\left(\frac{prf}{Hz}\right) + 20 \log(N)$$

Noise from the phase detector dominates the in-band noise floor, given here. The noise is in dBc/Hz

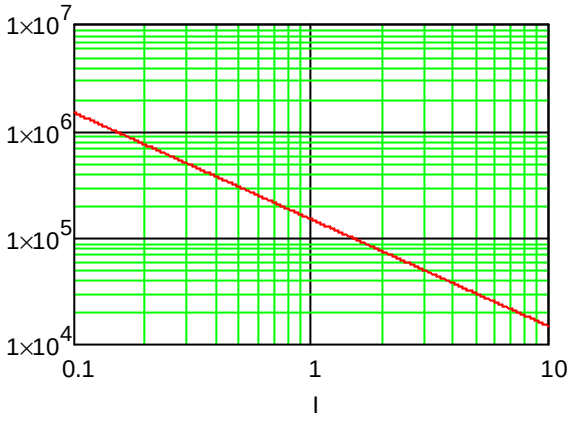
$InLoopPN(PDPN, 110) = -90.131$ dBc/Hz

Then calculate Fc.....

$$F_c(PNPD, N, Q_L, L, I_{bias}) := \frac{1}{\frac{2 \cdot Q_T(Q_L, L)}{f_o} \cdot \sqrt{\frac{10^{\left[\frac{(InLoopPN(PNPD, N))}{10}\right]}}{\left(\frac{2 \cdot F(Q_L, L) \cdot k_b \cdot T \cdot Hz}{P_s(Q_L, L, I_{bias})}\right)} - 1}}$$

$F_c(-203, 110, 10, 6.4nH, 1.5mA) = 99.4317 \cdot kHz$

$F_c(-203, 110, 10, 6.6nH, ImA)$



The integrated RMS phase noise in degrees is a very useful single-figure measure of performance and can be calculated using equations from page 50 of Deans book assuming a certain amount of peaking given in dB.

Peaking := 1

$$C(PNPD, N) := \frac{180}{\pi} \cdot 10^{\left(\frac{InLoopPN(PNPD, N)}{20}\right)}$$

$$RMSnoise(PNPD, N, Q_L, L, I_{bias}) := C(PNPD, N) \cdot \left[\sqrt{\left[\frac{F_c(PNPD, N, Q_L, L, I_{bias})}{Hz} \cdot \left(1 + 10^{\frac{Peaking}{10}}\right)\right] + \left(10^{\frac{Peaking}{10}} \cdot 2\right)}\right] \cdot de$$

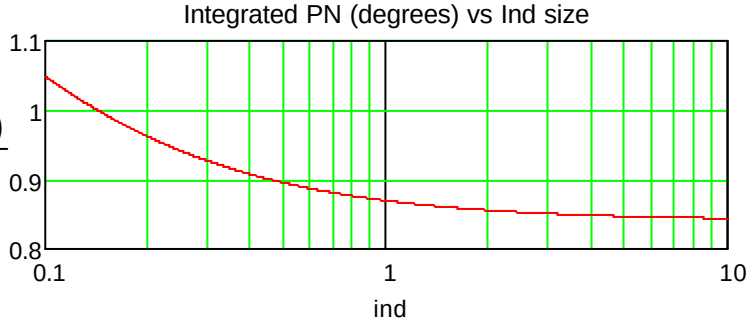
These results are interesting as they show that the total integrated-phase-noise, in a properly designed synth varies with CURRENT, Q, and N but not much with INDUCTANCE.

High Current, High Q, Low N

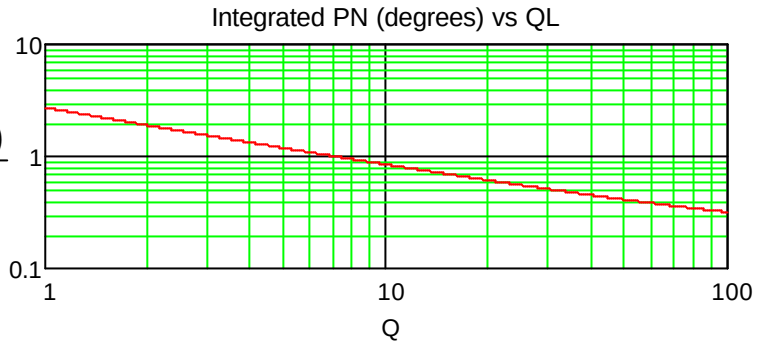
$\frac{RMSnoise(-203, 110, 10, 6.4 \cdot nH, 1.5mA)}{deg} = 0.846$

$\frac{RMSnoise(-203, 110, 10, 6.4 \cdot nH, 0.5mA)}{deg} = 1.465$

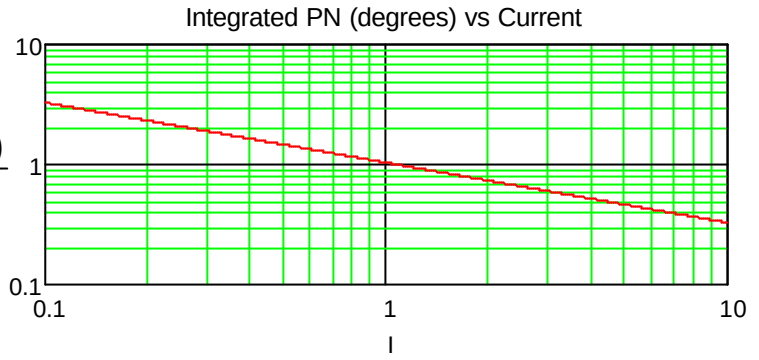
$\frac{RMSnoise(-203, 110, 10, ind \cdot nH, 1.5mA)}{deg}$



$$\frac{\mathrm{RMSnoise}(-203, 110, Q, 6.4\cdot nH, 1.5mA)}{\mathrm{deg}}$$



$$\frac{\mathrm{RMSnoise}(-203, 110, 10, 6.4\cdot nH, I mA)}{\mathrm{deg}}$$



$$\frac{\mathrm{RMSnoise}(-203, Div, 10, 6.4\cdot nH, 1.5mA)}{\mathrm{deg}}$$