

VCO & Synthesiser Design Sheet

This sheet is a useful general purpose design sheet for LC VCOs and PLLs. The topic is fairly complicated and choices made in the VCO design affect the PLL loop filter settings.

Start by entering the VCO components assuming a Colpitts topology.

Then calculate the effective VCO Q

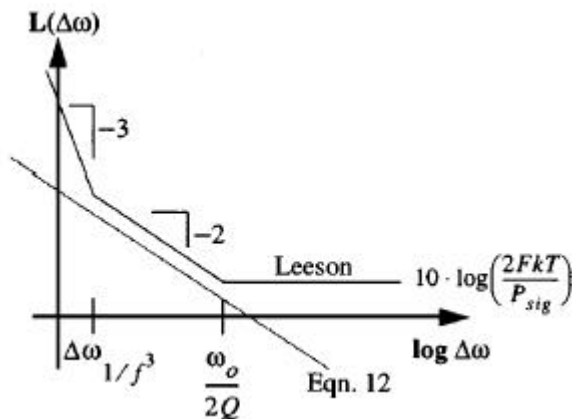
Then calculate the VCO phase noise profile,

Then the loop bandwidth and the integrated phase noise.

I will try to put some simulation results in soon, but at the moment this looks ok to me.

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<http://www.sunshadow.co.uk/chris.htm>



$$k_b := 1.388 \cdot 10^{-23} \frac{\text{joule}}{\text{K}} \quad T := 270 \cdot \text{K}$$

$$fF := 10^{-15} \cdot \text{farad} \quad \text{mW} := 10^{-3} \text{ watt} \quad \text{nH} := 10^{-9} \cdot \text{henry}$$

VCO Details, QC is Q for the Capacitor which is assumed to be high compared to the L, The VCO is assumed to be Colpitts.

$$f_o := 1.76 \cdot 10^9 \cdot \text{Hz}$$

$$Q_C := 200$$

VCO noise factor F

First calculate the noise factor (F) of the VCO transistor as defined by Rogers & Plett, Radio Freq Integrated Circuit Design (page 286), where **Rp** is the equivalent parallel resistance of the tuned circuit. Note that increasing the oscillator Q increases the noise floor.... not many people know that !!!

The noise equations are from Gray & Meyer page 752 and 759

Rb is the transistor bias resistor (Rogers p 271), assume 1V drop at 1mA = 1kohm

Rp is the effective parallel resistor of the VCO tuned circuit

and the higher this is, the higher the VCO **wideband** phase-noise, but the better close in phase noise.

$$R_b := 10000 \cdot \text{ohm}$$

$$i_{\text{biasnoise}} := \sqrt{\frac{4 \cdot k_b \cdot T \cdot \text{Hz}}{R_b}}$$

$$C(L) := \frac{1}{(2 \cdot \pi \cdot f_o)^2 L}$$

$$R_C(L) := \frac{Q_C}{2 \cdot \pi \cdot f_o \cdot C(L)}$$

$$i_{\text{biasnoise}} = 1.224 \times 10^{-12} \text{ amp}$$

$$R_L(Q_L, L) := Q_L \cdot L \cdot 2 \cdot \pi \cdot f_o$$

$$R_p(Q_L, L) := \frac{1}{\frac{1}{R_L(Q_L, L)} + \frac{1}{R_C(L)}}$$

$$C(6.4\text{nH}) = 1 \times 10^3 \text{ fF}$$

$$R_p(10, 6.4\text{nH}) = 674.036 \times 10^0 \Omega$$

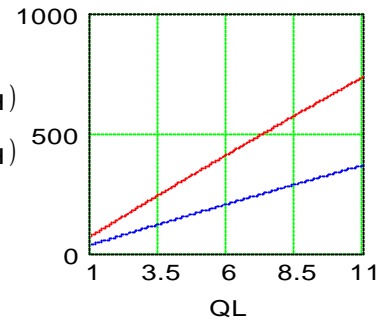
$$\rho := 0.5$$

$$g_m := 50 \frac{\text{mA}}{\text{volt}}$$

$$i_{\text{transistor}} := \sqrt{4 \cdot k_b \cdot T \cdot \frac{2}{3} \cdot g_m \cdot \text{Hz}}$$

$$R_p(Q_L, 6.4\text{nH})$$

$$R_p(Q_L, 3.2\text{nH})$$



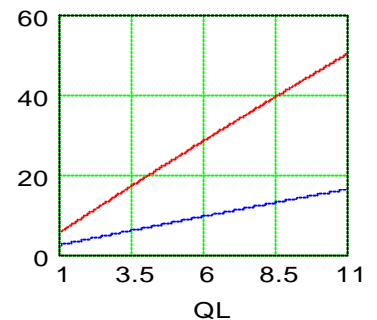
$$F(Q_L, L) := 1 + \frac{i_{\text{biasnoise}}^2 \cdot R_p(Q_L, L) \cdot \rho}{k_b \cdot T \cdot \text{Hz}} + \frac{i_{\text{transistor}}^2 \cdot R_p(Q_L, L) \cdot (1 - \rho)}{k_b \cdot T \cdot \text{Hz}}$$

$$10 \log(F(10, 6.4\text{nH})) = 16.6$$

This plot on the right shows the effective noise figure of the VCO under different QL, and inductor values. It also takes into account the bias resistance and the transistor gm, but NOT the transistor noise. The noise figure can be surprisingly high, but this affects the **wideband** phase noise only (noisefloor).

$$F(Q_L, 6.4\text{nH})$$

$$F(Q_L, 2\text{nH})$$



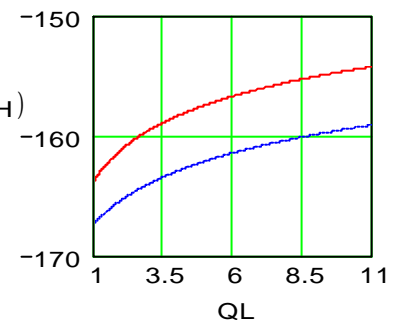
$$\text{Noisefloor}(Q_L, L) := 10 \cdot \log \left(2 \cdot T \cdot F(Q_L, L) \cdot k_b \cdot \frac{1}{\text{joule}} \right) + 30$$

$$\text{Noisefloor}(10, 6.4\text{nH}) = -154.6$$

Noise Floor in dBm

$$\text{Noisefloor}(Q_L, 6.4\text{nH})$$

$$\text{Noisefloor}(Q_L, 2\text{nH})$$



Oscillator Phase Noise

Now that we have the noise floor, the phase noise can be found from Rogers & Plett, Radio Freq Integrated Circuit Design (page 286), equation 8.90 and adding the affect for noise floor but ignoring flicker noise.

Qt = Q of Oscillator tank

Vtank = peak voltage swing in LC

Ps = power in loop (assumed to be output power)

PN is relative phase noise in dB

$$Q_T(Q_L, L) := R_p(Q_L, L) \cdot \sqrt{\frac{C(L)}{L}}$$

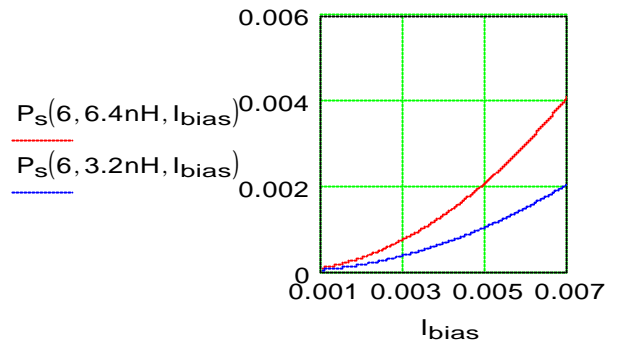
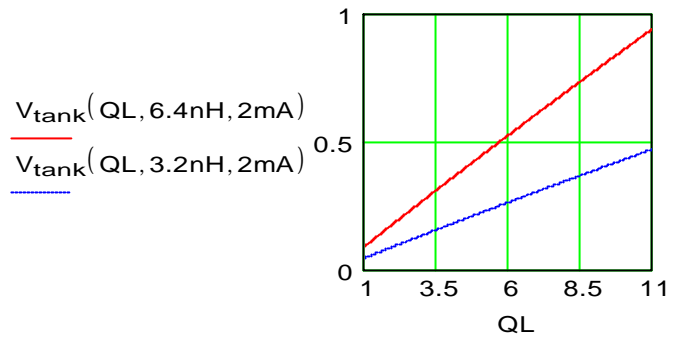
$$Q_T(10, 6.4\text{nH}) = 9.524$$

$$V_{\text{tank}}(Q_L, L, I_{\text{bias}}) := \frac{2}{\pi} \cdot I_{\text{bias}} \cdot R_p(Q_L, L)$$

$$V_{\text{tank}}(10, 6.4\text{nH}, 1.5\text{mA}) = 0.64 \text{ volt}$$

$$P_s(Q_L, L, I_{\text{bias}}) := \frac{V_{\text{tank}}(Q_L, L, I_{\text{bias}})^2}{2 \cdot R_p(Q_L, L)}$$

$$P_s(10, 6.4\text{nH}, 1.5\text{mA}) = 0.307 \text{ mW}$$



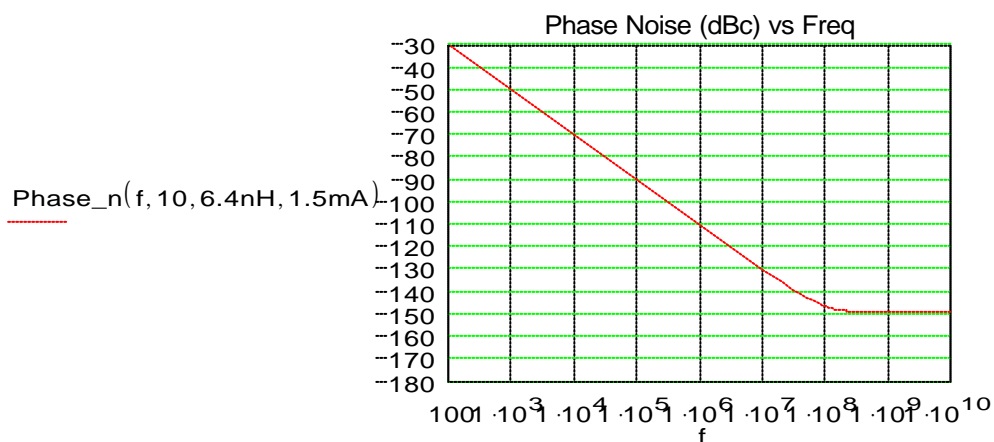
The VCO output power is **assumed** to be a **quarter** the power in the loop (P_s).

This calculates the phase noise according to the Leeson's equation assuming the phase-noise is dominated by the Q, i.e the noise slope is 20dB/decade.
 This plot will have the same wideband noise floor as specified above (in dBm)
if P_s (above) is set to $4 * 1\text{mW}$.

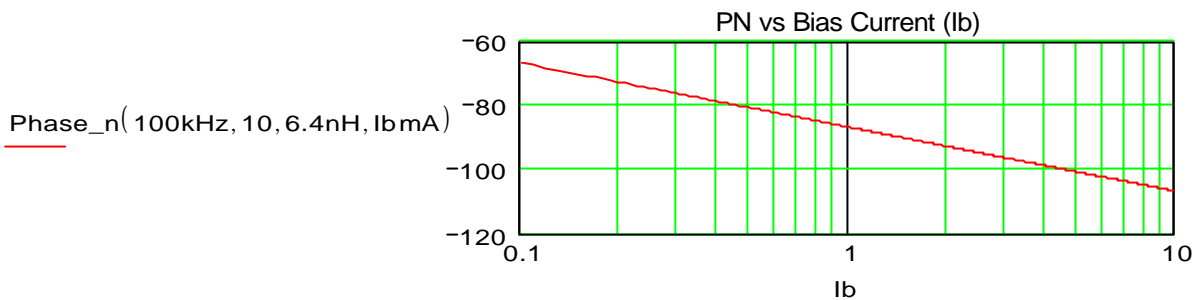
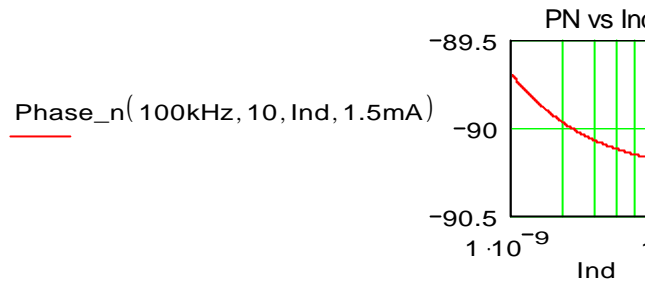
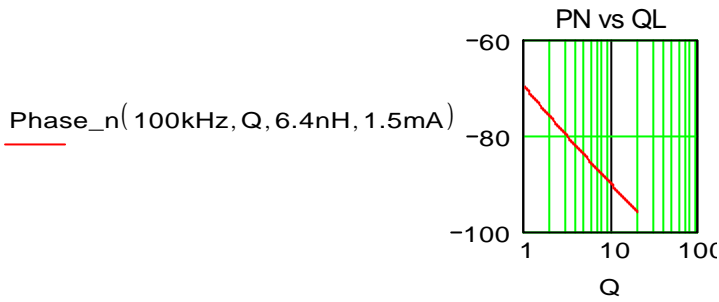
The phase noise is in dBc

$$\text{Phase}_n(\Delta f, Q_L, L, I_{\text{bias}}) := 10 \cdot \log \left[1 + \left(\frac{f_0}{2 \cdot Q_T(Q_L, L) \cdot \Delta f} \right)^2 \frac{2F(Q_L, L) \cdot k_b \cdot T \cdot \text{Hz}}{P_s(Q_L, L, I_{\text{bias}})} \right]$$

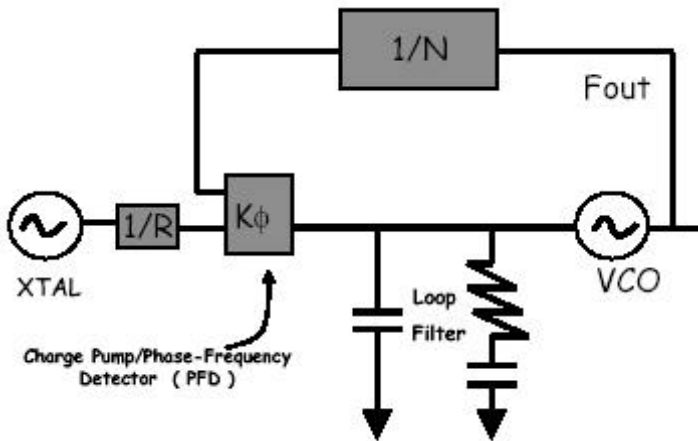
$\text{Phase}_n(100 \cdot \text{kHz}, 10, 6.4\text{nH}, 1.5\text{mA}) = -90.2$ $\text{Phase}_n(500 \cdot \text{MHz}, 10, 6.4\text{nH}, 1.5\text{mA}) = -149.3$ dBc



These plots show how the phase noise changes.
 There are only two ways to improve the phase noise, increase Q and increase current.



Next, design the Synth for Minimum Phase Noise...



The phase noise calculation inside a synth loop is found from the Deans Book from Nat Semi

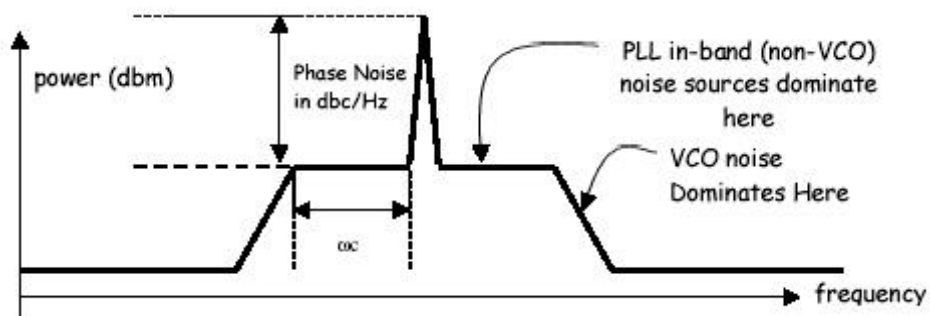
The Phase detector phase noise (PDPN) is guessed at and is in dBm/Hz, The limit is typically -207 prf is the phase-reference-freq

$N := 110$

$PDPN := -203$

$prf := \frac{f_o}{N}$

$prf = 16.0\text{MHz}$



This part calculates the PLL in-band phase-noise in -dBc/Hz. F_c is designed to be the point where the VCO noise and the in-loop phase noise are the same as this will minimise the total Phase Noise out of the synth.

First we need to calculate the in-loop phase noise from **PNPD** (phase noise of the phase detector).

$$\text{InLoopPN}(\text{PDPN}, N) := \text{PDPN} + 10 \cdot \log\left(\frac{\text{prf}}{\text{Hz}}\right) + 20 \log(N)$$

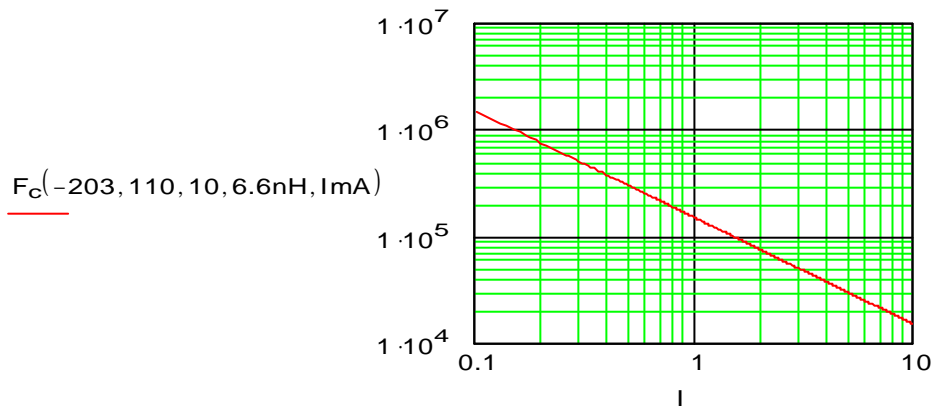
Noise from the phase detector dominates the in-band noise floor, given here. The noise is in dBc/Hz

$$\text{InLoopPN}(\text{PDPN}, 110) = -90.131 \text{ dBc/Hz}$$

Then calculate F_c

$$F_c(\text{PNPD}, N, Q_L, L, I_{\text{bias}}) := \frac{1}{\frac{2 \cdot Q_T(Q_L, L)}{f_o} \cdot \sqrt{\frac{10^{\frac{(\text{InLoopPN}(\text{PNPD}, N))}{10}}}{\left(\frac{2 \cdot F(Q_L, L) \cdot k_b \cdot T \cdot \text{Hz}}{P_s(Q_L, L, I_{\text{bias}})}\right) - 1}}}$$

$$F_c(-203, 110, 10, 6.4\text{nH}, 1.5\text{mA}) = 99.4317 \text{ kHz}$$



The integrated RMS phase noise in degrees is a very useful single-figure measure of performance and can be calculated using equations from page 50 of Deans book assuming a certain amount of peaking given in dB.

Peaking := 1

$$C(\text{PNPD}, N) := \frac{180}{\pi} \cdot 10^{\left(\frac{\text{InLoopPN}(\text{PNPD}, N)}{20}\right)}$$

$$\text{RMSnoise}(\text{PNPD}, N, Q_L, L, I_{\text{bias}}) := C(\text{PNPD}, N) \cdot \sqrt{\left[\frac{F_c(\text{PNPD}, N, Q_L, L, I_{\text{bias}})}{\text{Hz}} \cdot \left(1 + 10^{\frac{\text{Peaking}}{10}}\right)\right] + \left(10^{\frac{\text{Peaking}}{10}} \cdot 2\right)}$$

These results are interesting as they show that the total integrated-phase-noise, in a properly designed synth varies with CURRENT, Q, and N but not much with INDUCTANCE.

High Current, High Q, Low N

$$\frac{\text{RMSnoise}(-203, 110, 10, 6.4 \cdot \text{nH}, 1.5\text{mA})}{\text{deg}} = 0.846$$

$$\frac{\text{RMSnoise}(-203, 110, 10, 6.4 \cdot \text{nH}, 0.5\text{mA})}{\text{deg}} = 1.465$$

