

Plot of Signal/Noise against ADC/DAC quantisation (n) for Sinusoidal Modulation

Simon Haykin, Comms Systems & VLSI Handbook

Chris Haji-Michael
<http://www.sunshadow.co.uk/chris.htm>

M := 4

M = Oversampling Ratio = Fs/2B.

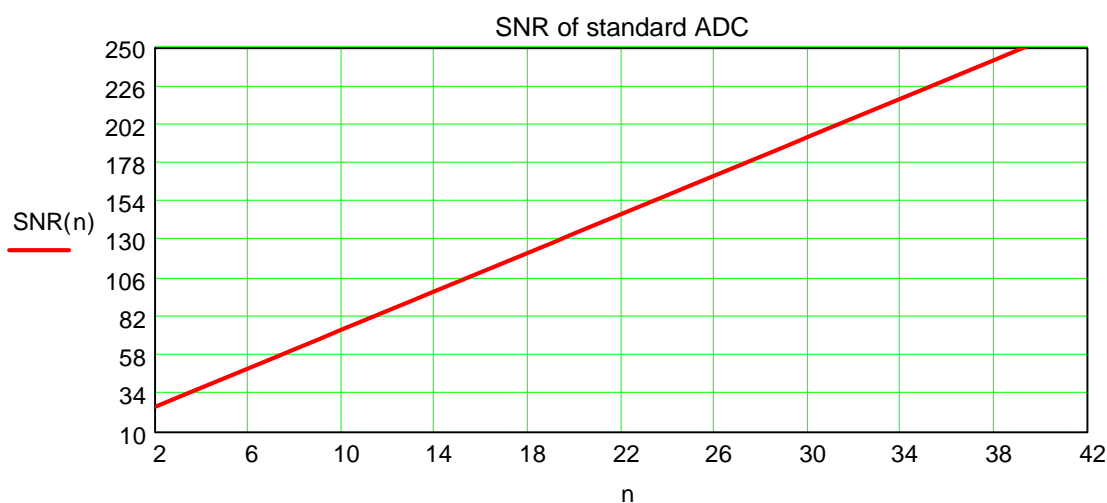
The noise power is spread over the full bandwidth, whereas if the signal is oversampled, (i.e. more than the Nyquist limit of twice) then the noise power decreases by 6dB for each doubling.

n := 2..45

n is resolution in number of bits

$$SNR(n) := 10 \cdot \log \left[\frac{3}{2} \cdot (2^{2 \cdot n}) \right] + 20 \log(M)$$

SNR of standard ADC or DAC

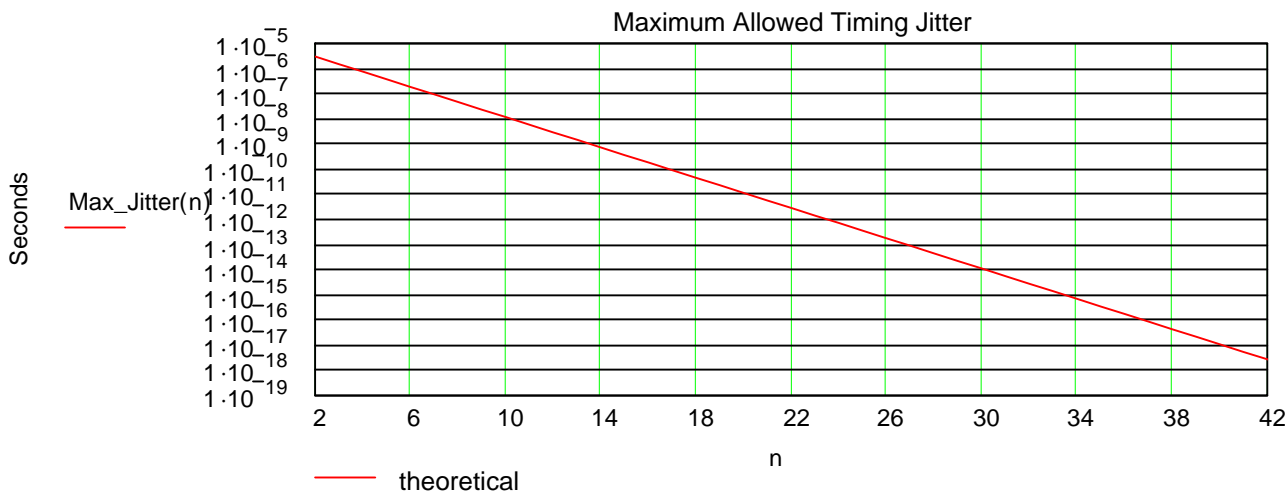


B := 22kHz

B = Bandwidth of wanted signal

$$Max_Jitter(n) := \frac{1}{2 \cdot \pi \cdot B \cdot 2^n} \left(\frac{2M}{3} \right)^{0.5}$$

The Max_Jitter is the maximum allowed clock jitter for the ADC to perform to spec. It is a function of the bandwidth B and the oversampling ratio M



This page plots the SNR of an oversampled delta-sigma ADC or DAC.

The oversampling, usually at many times the nyquist rate and the use signal processing techniques increase the effective quantisation. It amazes me that a good SNR that can be achieved with low quantisation but high sampling.

The key different parameter is L which is the modulator order.

When L = 1, the error in the next signal is taken as being the error measured in the previous. This is ok for exceedingly slow signals.

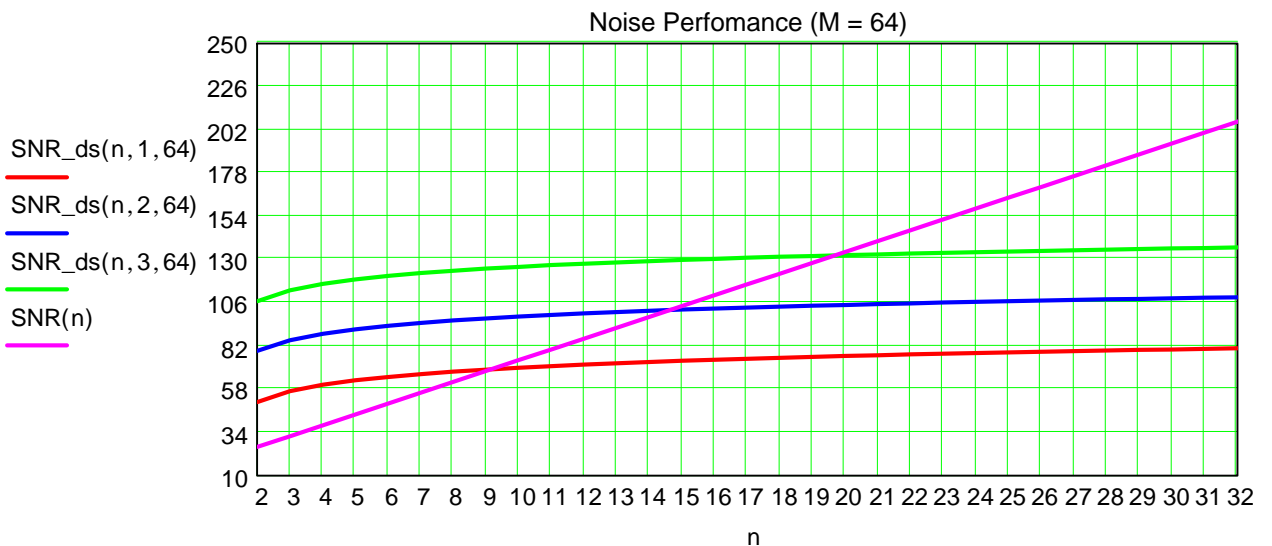
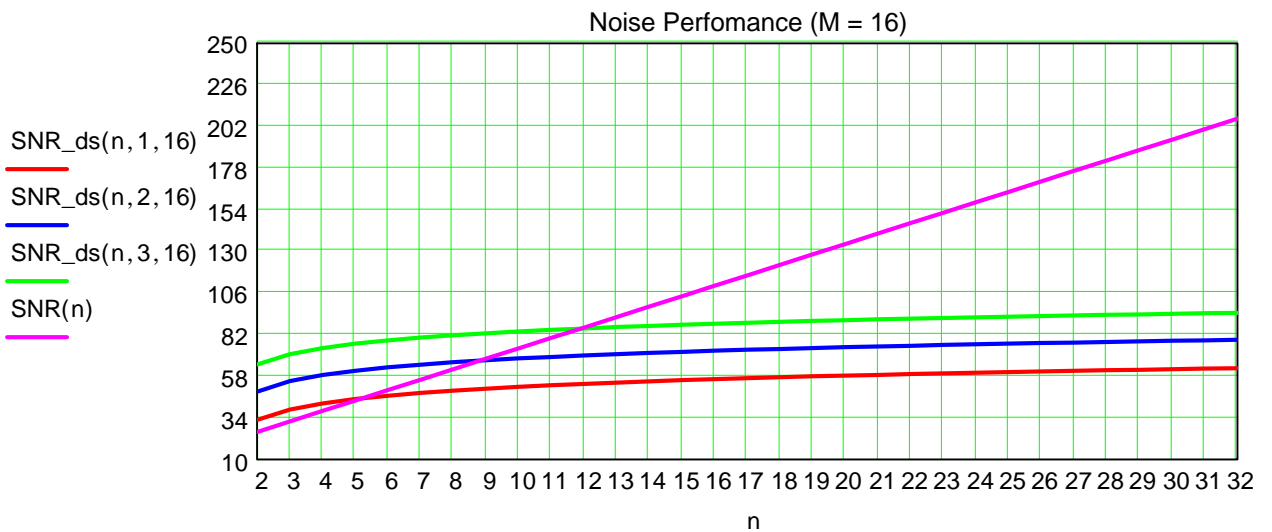
When L = 2, the error is assumed to vary linearly.

M = Oversampling Ratio, set for much higher for delta-sigma converter

L := 1, 2.. 6

Mds := 8, 16.. 512

$$\text{SNR_ds}(n, L, \text{Mds}) := 10 \cdot \log \left[\frac{3}{2} \cdot \left(\frac{2 \cdot L + 1}{\pi^{2 \cdot L}} \right) \text{Mds}^{2 \cdot L + 1} \cdot (n - 1)^2 \right]$$



Noise Performance (M = 512)

