Masters Thesis

Design of a Lossless Feedback Amplifier Using a 0.25μm CMOS Process

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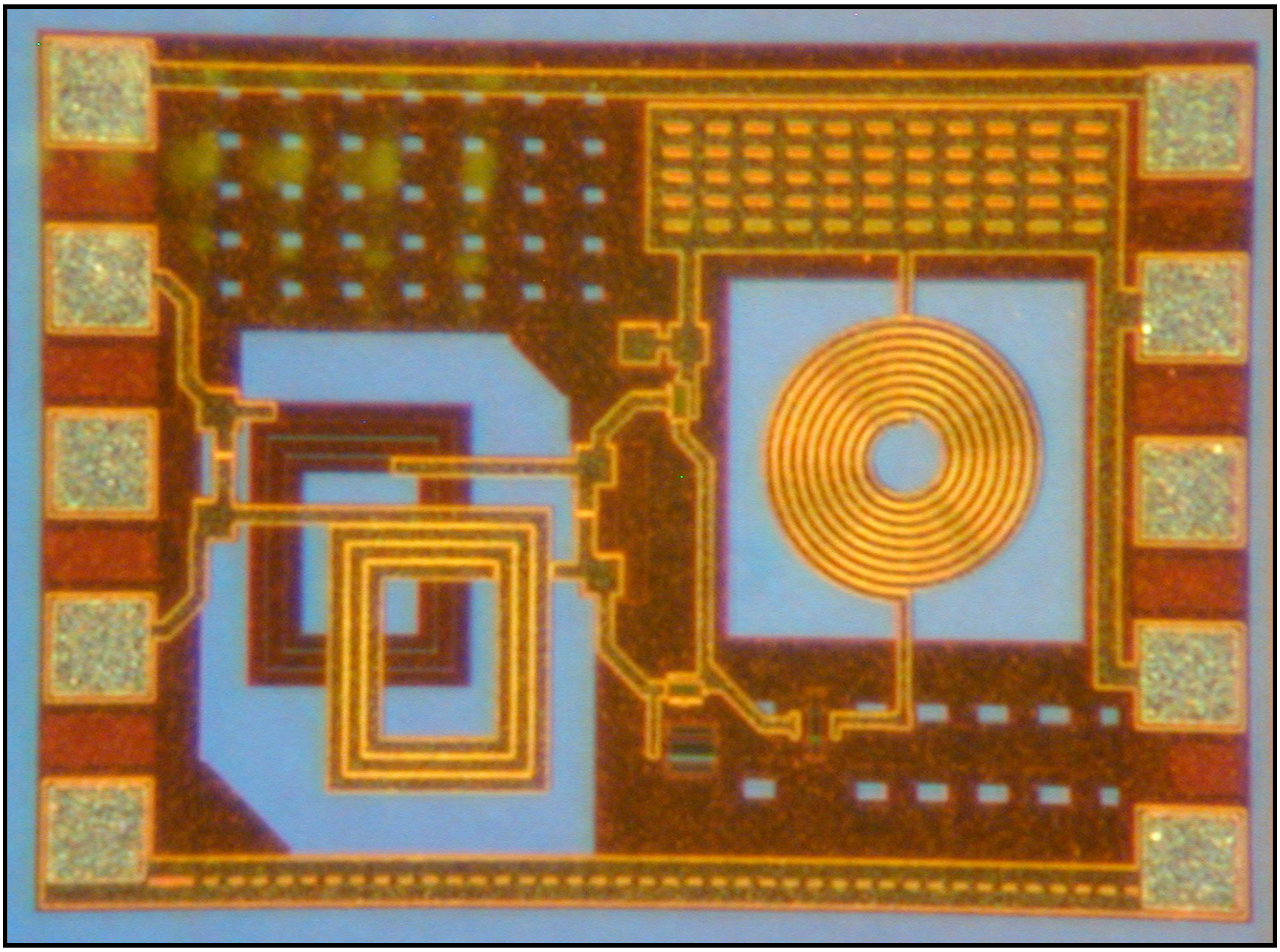

PREFACE

The Thesis investigates three circuit blocks for their suitability for fabrication on an IC. It investigates two types of RF Directional Coupler and combines one of these with a gain-block to build an amplifier topology referred to as a Lossless-Feedback or Norton Amplifier.

The design procedure for each of these circuit blocks is presented in the Thesis. A paper describing the design of one of the RF Directional Couplers has been written and submitted for publication. Test results for the Norton Amplifier look promising, but an IC fabrication error prevents direct comparison between the simulated and measured results and as a consequence it has not been possible to submit a paper on this. The IC is currently being re-fabricated but it has not been returned in time for testing. The second RF Directional Coupler was less successful, but using the information gathered during testing, this has been re-designed and I hope the University takes the opportunity to have this rebuilt, as it is an interesting and useful circuit that could see many applications.

A CD is attached on the back page of this Thesis that contains an electronic copy of this document with hyperlinks to many of the references. It also includes the LabVIEW scripts, MathCAD files, ADS simulation files, results data and Cadence layout files used in this Thesis.

I would like to take this opportunity to thank the staff in the RISC group at Aalborg University for allowing me to return to study and to give me this opportunity to learn the techniques for designing and testing an RFIC. I am very grateful for this and for all their help, especially the PhD students who answered all my many questions. I would specifically like to thank my supervisor Ole Kiel Jensen for his invaluable comments, and to RFMD for the use of one of their machines that I needed during the testing.

The fabrication process used in this Thesis is from UMC and they have demanded confidentiality of their process. As a consequence this Thesis should not be made available to unauthorized readers.

Thank you,

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1 INTRODUCTION

1.1 Project Outline

The aim of this project is to investigate and design a type of amplifier referred to as lossless feedback amplifier with regard to its suitability for use in an integrated circuit design.

The use of feedback around an amplifier has been used for many years to control and improve amplifier performance. Several factors are known to change when feedback is used, of which linearity and noise-figure are the two main factors investigated as part of this report. The normal method of adding feedback to an amplifier is to use resistive components, but these add noise and degrade the amplifier noise figure. It is however possible to employ reactive components in the feedback path and to enjoy the advantages of improved linearity but with a minimal degradation to the amplifier noise figure. Such an amplifier was first proposed and patented by D. Norton [1] of the Anzac Corporation, with the basic structure of this type of amplifier shown in Figure 1.1. Amplifiers of this type are referred to as Norton amplifiers, and were sold operating to typically 200MHz.

It is the intention of this project to design and build a Norton amplifier that operates at 2GHz on a CMOS process. This type of amplifier has to the authors knowledge not been built on an IC before and there are no published papers to give guidance on the approach that should be taken. In addition, a suitable coupler required to provide the necessary coupling has also not been built, although the design of a 3dB hybrid was published in March 2003 by Frye [2] and is used as a starting point for this design.

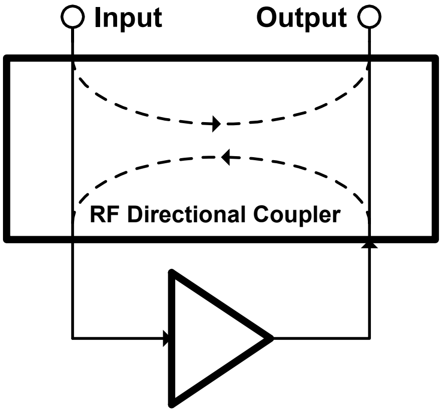


Figure 1.1 – Block Diagram of Lossless Feedback Amplifier Using an RF directional coupler as the feedback path.

This thesis starts by investigating suitable couplers; with the design choices for these and the gain-block presented in Chapter 2. The IC construction is explained in Chapter 3 and this also includes information on the simulation and layout of the passive components.

Two couplers and the Norton amplifier were selected for fabrication and the test results for these are presented in Chapter 5. The test results show that the amplifier and one of the couplers is successful and show good correlation between the simulated and measured results. The results for the second coupler do not agree with the simulations and this is investigated as part of Chapter 5. An updated design for the second coupler is presented in Chapter 6.

The results in Chapter 5 (Figure 5.13) show that the amplifier achieves a 10dB increase in IIP3 over the frequency band 1.5 to 2GHz and this is the first time that such an amplifier has been demonstrated. An updated amplifier with biasing is presented in Chapter 6.

1.2 Definition and Explanation of terms

1.2.1 Amplifier Linearity

A receiver picks up a variety of signals from the antenna at different power levels and frequencies and in amongst these is the wanted signal. The receiver must be able to amplify and demodulate this signal, usually at a very low power level in the presence of the other signals that are often at much higher power levels.

Non-linearities in the receiver chain can prevent this from happening. Mixing affects allow two unwanted frequencies to mix together to generate a number of spurious signals. If one of these unwanted spurious signals falls at the frequency of interest, it will affect the demodulator performance and this will result in a degraded signal to noise ratio.

A clear way to explain this affect is mathematically. The mixing products generated by two signals can be expressed as a Taylor series expansion in terms of the input voltage v_i and where v_o is the output voltage. In this analysis the input voltage is made up of two closely spaced frequencies ω_1 and ω_2 as follows.

$$v_i = V_0 \cdot \left(\cos \omega_1 t + \cos \omega_2 t\right)$$

The output voltage can be expressed as follows after expansion of the Taylor Series:

$$\begin{aligned} v_0 = {} & \alpha_0 + \alpha_1 V_0 \left(\cos \omega_1 t + \cos \omega_2 t\right) + \alpha_2 V_0^2 \left(\cos \omega_1 t + \cos \omega_2 t\right)^2 \\ & + \alpha_3 V_0^3 \left(\cos \omega_1 t + \cos \omega_2 t\right)^3 + \ldots \end{aligned}$$

Which becomes:

$$\begin{aligned} v_0 = {} & \alpha_0 + \alpha_1 V_0 \cos \omega_1 t + \alpha_2 V_0 \cos \omega_2 t \\ & + \tfrac{1}{2} \alpha_2 V_0^2 (1 + \cos 2\omega_1 t) + \tfrac{1}{2} \alpha_2 V_0^2 (1 + \cos 2\omega_2 t) \\ & + \alpha_2 V_0^2 \cos(\omega_1 - \omega_2) t + \alpha_2 V_0^2 \cos(\omega_1 + \omega_2) t \\ & + \alpha_3 V_0^3 \left(\tfrac{3}{4} \cos \omega_1 t + \tfrac{1}{4} \cos 3\omega_1 t\right) + \alpha_3 V_0^3 \left(\tfrac{3}{4} \cos \omega_2 t + \tfrac{1}{4} \cos 3\omega_2 t\right) \\ & + \alpha_3 V_0^3 \left(\tfrac{3}{2} \cos \omega_2 t + \tfrac{3}{4} \cos(2\omega_1 - \omega_2) t + \tfrac{3}{4} \cos(2\omega_1 + \omega_2) t\right) \\ & + \alpha_3 V_0^3 \left(\tfrac{3}{2} \cos \omega_1 t + \tfrac{3}{4} \cos(2\omega_2 - \omega_1) t + \tfrac{3}{4} \cos(2\omega_2 + \omega_1) t\right) + \ldots \end{aligned}$$

The combination of ω_1 and ω_2 are called the *intermodulation products*. The V_0^2 terms from the above equation is referred to as the *second order term,* of which there are four: $2\omega_1$, $2\omega_2$, $\omega_1 - \omega_2$ and $\omega_1 + \omega_2$. A simple way to categorize these is to define the output as $m\omega_1 + n\omega_2$, where the order is defined as $|m| + |n|$. The second order frequency products are listed in Table 1.1, and in a similar way the third order products can be listed for V_0^3 terms; of which there are six. These terms are listed in Table 1.2.

All the products generated by an amplifier are undesirable, however the spurious signals that are generated some distance away from the wanted signal can be easily filtered out before the mixer and should present no great challenge in the receiver design. The products that present the greatest cause for concern are the adjacent spurious signals $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, as these are too close to the wanted signal to be filtered out and can only be controlled by designing the amplifier to be sufficiently linear.

Order	m	n	Spurious	Description
2	2	0	$2\omega_1$	Second harmonic of ω_1
2	0	2	$2\omega_2$	Second harmonic of ω_2
2	1	-1	$\omega_1 - \omega_2$	Difference
2	1	1	$\omega_1 + \omega_2$	Sum

Table 1.1 - Second Order Intermodulation Terms

Order	m	n	Spurious	Description
3	3	0	$3\omega_1$	Third harmonic of ω_1
3	0	3	$3\omega_2$	Third harmonic of ω_2
3	2	-1	$2\omega_1 - \omega_2$	Low side adjacent spurious
3	-1	2	$2\omega_2 - \omega_1$	High side adjacent spurious
3	2	1	$2\omega_1 + \omega_2$	
3	1	2	$2\omega_2 + \omega_1$	

Table 1.2 – Third Order Intermodulation Terms

A spectrum showing only the second and third-order terms can be seen in Figure 1.2, this shows that most mixing products are some distance away from ω_1 and ω_2. A typical receiver is shown in Figure 1.3, one of the advantages for putting a filter between the first amplifier and the mixer is to remove these unwanted mixing products. This filter however cannot remove the adjacent channel spurious signals and it is an important specification for the LNA design is to be sufficiently linear so as not to generate these unwanted spurious signals in the operating environment.

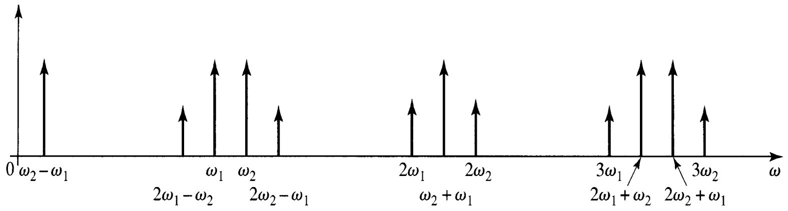


Figure 1.2 – Output Spectrum of 2nd and 3rd-order Intermodulation Products [3]

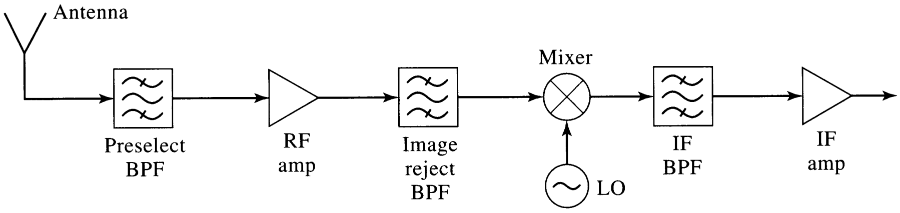


Figure 1.3 – Typical Receiver Topology [3]

1.2.2 Third-Order Intercept Point

The LNA linearity is conveniently measured using the *third-order Intercept Point*. The mixing product from two unwanted signals increases as a cube of the input power. For small signals the third-order intermodulation products will be small but will increase quickly as the input power increases. This effect can be seen in Figure 1.4 where the first and third-order output products are plotted against the input power. The scales on both axes are logarithmic and it can be seen from this graph that this device shows a gain of 30dB and that the fundamental signal increases linearly until the output power compresses at 20dBm.

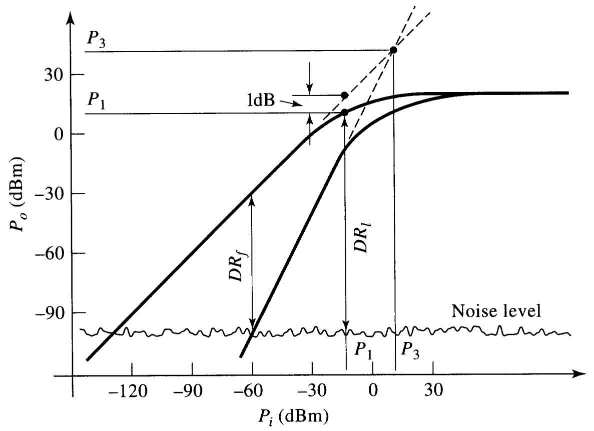


Figure 1.4 – Third Order Intercept Diagram [3]

The third order products increase at a slope of three, since the fundamental and third order products have different slopes they intersect at a point that is referred to as the *Third Order Intercept Point*, shown as P3 in Figure 1.4. Either the input or output intercept points are acceptable to define the amplifier linearity and it is easy to switch between the two points by adding or subtracting the amplifier gain.

To maintain consistency and simplicity in comparing the different amplifiers, this report uses only the *input* third order intercept point, written as IIP3, but which may also be written as TOIi. This report uses IIP3 throughout and allows a direct comparison with published literature [please refer to chapter 1.5].

The unwanted frequencies used for this measurement are typically between ±200kHz and ±2 MHz from the wanted signal. As an example for the GSM spec [4] the unwanted intermodulation frequencies for GSM900 are set to ±800kHz and ±1600kHz, at –49dBm. These unwanted signals must not degrade the performance of the receiver demodulating the wanted signal, which is set to 3dB above the reference sensitivity to –101dBm. Assuming the unwanted spurious level needs to be 6dB below the wanted signal to have little influence on the receive BER, i.e. a power level of less than –107dBm, then the IIP3 of the receiver can be calculated from the equation below.

$$IIP3 = UnwantedSignalLevel + \frac{1}{2}(UnwantedSignalLevel - SpuriousLevel)$$

using values from the GSM spec:

$$IIP3 = -49dBm + \frac{1}{2}(-49dBm - -107dBm)$$

this gives an:

$$IIP3 = -20dBm$$

This equation gives a good insight as to the benefit that may be obtained by an improvement in the receiver IIP3. A 10dB improvement in the IIP3 indicates that the spurious signal levels will have fallen by 20dB.

1.2.3 1dB Compression Point

Another measure of linearity is the 1dB compression point, which is measured using a single input CW frequency. The response of a typical amplifier is shown in Figure 1.5; for an ideal linear amplifier a plot of the output power versus the input power is a straight line with a slope of unity. In this figure the gain of the amplifier is 10dB but as the input power increase the output saturates reducing the gain. The output power at which the gain drops 1dB below the expected value is referred to as the 1dB compression point and is always referenced to the output of the amplifier, it is written as *P1dB*.

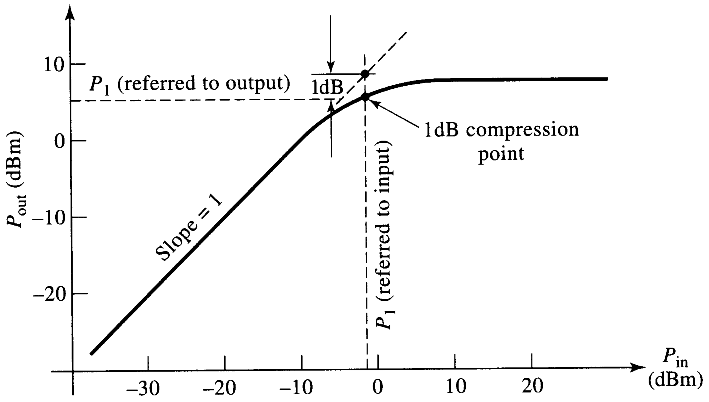


Figure 1.5 – 1dB Compression Point [3]

1.2.4 AM to PM conversion

When an amplifier is driven close to its compression point, a change in the amplitude of the input signal can result in a change in the phase. This is known as the AM to PM conversion and needs to be seriously considered with RF systems that transmit or receive certain types of modulation, and is another description of amplifier linearity.

The effect is most important when the modulation has both an amplitude and phase component for example with QAM signals. A 16-bit QAM constellation is shown in Figure 1.6 and has 16 points, each with a unique amplitude and phase. If this signal is amplified using an amplifier with a poor AM-PM conversion then the amplifier will distort the signal such that the outer constellation points have a different phase shift compared to the inner constellation points and this will result in a degraded system BER and increased output harmonics.

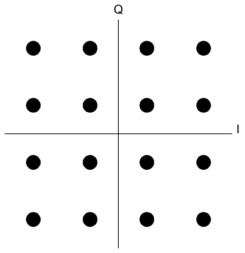


Figure 1.6 – 16-QAM Signal Constellation

1.2.5 Stability

Adding feedback to an amplifier increases the chance that the amplifier will become unstable, as stability depends on the gain and phase of *all* the parts in the circuit. The standard method of assessing the stability of an amplifier is to calculate the *Rollet's* stability measure using the amplifier S-parameter data. The *Rollet's* measure is calculated as shown below and two conditions need to be met for the amplifier to be considered unconditionally stable.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12}S_{21}|} > 1$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

Unconditional stability is when the circuit is stable and will not oscillate under *all* load and source impedances. The stability factor needs to be calculated at many frequencies over a wide frequency band and not just over the amplifier band of interest. An oscillation at *any* frequency is of concern and will degrade the performance of the amplifier usually influencing the amplifier noise figure and the gain. The typical bandwidth to apply this measure to is from a few megahertz up to $F_T/2$ frequency of the transistor. For the UMC process, stability is calculated up to 10GHz.

Other measures of stability that has become popular over recent years are μ and μ', as defined Edward and Sinsky [5]. These are the geometrically derived stability factors where μ is the stability factor for the load, and μ' is the stability factor for the source. These values give a simple measure of the distances from the center of the Smith chart to the nearest point of instability as shown using stability circles. Both of these values need to be greater than 1 for unconditional stability and the value given are directly proportional to degree of instability.

Part of the motivation behind the Edward and Sinsky method is that the Rollet's measure of stability is more complex than presented above. Stability requires K>1, and *any one* of the following conditions to apply, of which the most commonly used is $|\Delta|$.

$$\begin{aligned}
B_1 &= 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \\
B_2 &= 1 - |S_{11}|^2 + |S_{22}|^2 - |\Delta|^2 > 0 \\
|\Delta| &= |S_{11}S_{22} - S_{12}S_{21}| < 1 \\
&\quad 1 - |S_{11}|^2 > |S_{12}S_{21}| \\
&\quad 1 - |S_{22}|^2 > |S_{12}S_{21}|.
\end{aligned}$$

This makes the Rollet's analysis complex and difficult to appreciate how much margin there is in the design of a circuit. The stability measures of μ and μ' are easily calculated as shown below and both parts need to be >1 for unconditional stability. Both the Rollet's and μ & μ' indicators are all used in this report.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \cdot \Delta| + |S_{21} \cdot S_{12}|}$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \cdot \Delta| + |S_{21} \cdot S_{12}|}$$

1.2.6 Stability Circles

Stability Circles are a graphical method of showing the stability of an amplifier. The derivation of these circuits is complex and the reader is referred to Pozar [3] for more information. Stability circles are normally calculated for both the load (output) and source (input) impedances and show the impedances that are likely to cause the amplifier to become unstable.

The center and radius of these circles are calculated at each frequency according to the following equations. For simplicity these are given for the load impedance, but similar equations can be found for the source impedance. This circle can be plotted on a Smith chart as shown in Figure 1.7.

$$C_L = \frac{\left(S_{22} - \Delta \cdot S_{11}^*\right)^*}{\left|S_{ss}\right|^2 - \left|\Delta\right|^2}$$

$$R_L = \left|\frac{S_{12} \cdot S_{21}}{\left|S_{22}\right|^2 - \left|\Delta\right|^2}\right|$$

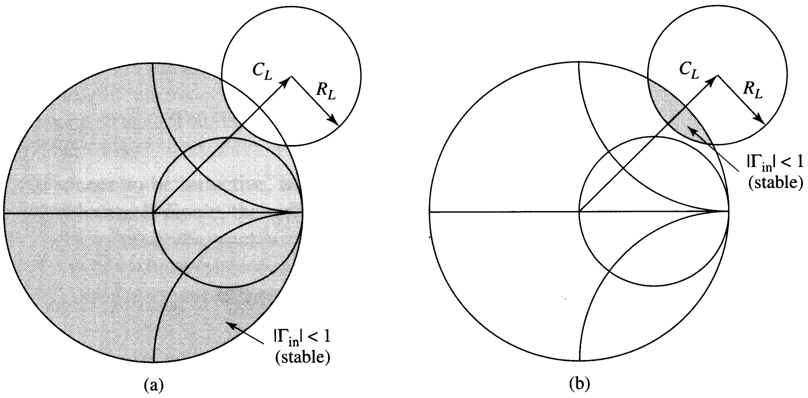


Figure 1.7 – Stability Circles [3]

If the amplifier is unconditionally stable, the stability circles must be completely outside or totally enclose the smith chart. One difficulty with interpreting stability circles is working out which region shows the stable impedances and which is the unstable region, as either condition shown in Figure 1.7 may be correct. There are two ways to do this, the first is to calculate $\left|S_{11}\right|$ and this is shown in Figure 1.7(a) is with $\left|S_{11}\right| < 1$ and Figure 1.7(b) is with $\left|S_{11}\right| > 1$. The second method is to use μ & μ' as the indicators.

1.2.7 Gain

The value of gain used throughout this report is $\left|S_{21}\right|^2$ which assumes the same port impedance on both the input and output ports.

1.2.8 Noise Figure

The amplifier adds noise to the signal such that the noise figure of the amplifier is a ratio of the input and output signals and noise powers as follows. This report expresses the Noise figure in dBs; $F(dB) = 10 \cdot Log(F)$.

1.3 Types of Lossless Feedback Amplifier

D Norton of the Anzac Corporation patented the first lossless-feedback amplifier in 1971 [1][6]. He proposed that a directional coupler could be used in the feedback path around the transistor and thereby improved the amplifier linearity but without substantially affecting the input and output impedance and the amplifier noise figure. This group of amplifiers is collectively referred to as *Norton* amplifiers.

In the patented configuration shown in Figure 1.8, two independent transformers are used to form a single directional coupler that has zero phase-shift between ports P4 and P2. Some of the output power from the transistor at P4 feeds back to the input port P2 at zero-phase thus creating a feedback path in much the same way as a resistive element could be used. The advantage is this mechanism should not introduce additional noise power that a corresponding resistor would introduce and should therefore not degrade the amplifier noise figure. In addition, the use of directional couplers allows the feedback mechanism to work without influencing the input or output impedance and these should remain unchanged.

With this topology for optimum performance, the base and collector impedance of the transistor should be the same as the impedance of the IN and OUT ports, so for a 50-Ohm amplifier the base and collector impedances should look like 50-Ohm.

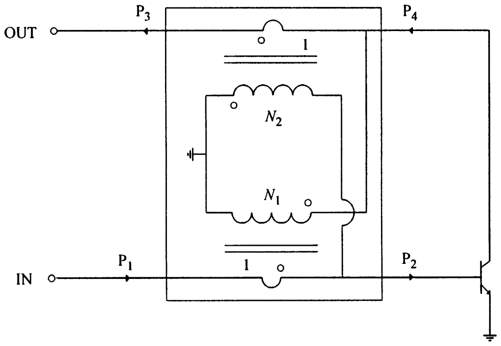


Figure 1.8 – D Norton Lossless Feedback Amplifier [6]

It is interesting to note with this circuit that some of the input power passes directly to the output port via the directional coupler and we should see some output power even if the transistor were not fitted. As the coupler is reciprocal the reverse of this must happen and a proportion of any power in the output port will be coupled directly to the input. This indicates that the reverse isolation of this type of amplifier is limited to coupling level of the coupler.

For some applications this may be a problem and this was solved in 1977 by Q-bit [7] using two directional-couplers instead of one. The topology for this amplifier is shown in Figure 1.9; in this arrangement any RF power incident on the output port is split between the transistor and a terminating load on P4. The reverse isolation of this topology is that of the transistor itself plus any losses associated with the couplers. The disadvantage is that there is slightly less output power, as part of the input power in the original design would contribute to the output power, in addition there is also increased losses using two couplers and the circuit is more complex.

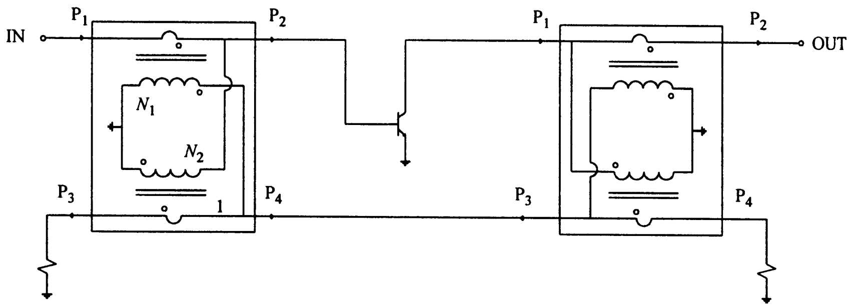

IN
P1
P2
N1
N2
P3
1
P4
P1
P2
OUT
P3
P4

Figure 1.9 - Q-Bit Norton Amplifier [6]

In 1975, D. Norton and A. Podel patented [8] another topology that uses a wound transformer in place of the directional couplers and works using a single transistor amplifier stage. In this circuit shown in Figure 1.10, for correct operation the input impedance of the transistor should approximate a short circuit, while the output impedance should look like an open circuit.

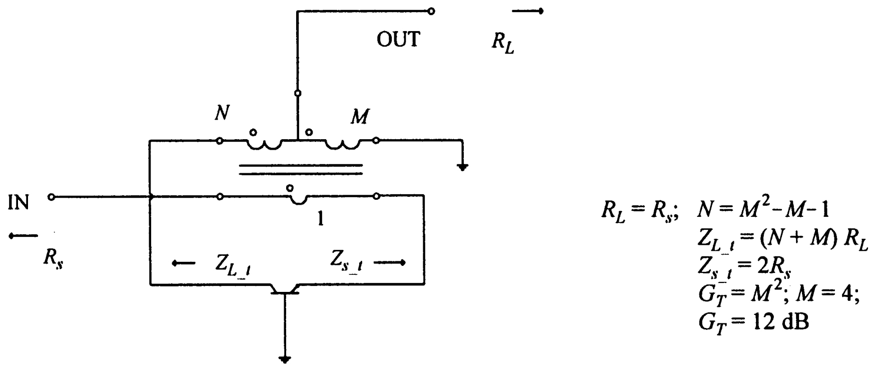

OUT
R_L
N
M
IN
R_s
1
Z_{L_t}
Z_{s_t}
$R_L = R_s$; $N = M^2 - M - 1$
$Z_{L\_t} = (N + M) R_L$
$Z_{s\_t} = 2R_s$
$G_T = M^2$; $M = 4$;
$G_T = 12$ dB

Figure 1.10 - Transformer Wound Norton Amplifier [6]

A different class of feedback amplifiers is the *transformer feedback amplifier* by Long and Copeland in 1995 [9]. The circuit they proposed is shown Figure 1.11 and uses a transformer with a 1 to 4 winding ratio to replace the collector and emitter impedances normally used in amplifier design. The design presented is tuned for narrow-band operation with the addition of a collector capacitor and has a number of matching off-chip components.

A 1.9GHz LNA was built using this topology on a 0.8um silicon process and biased at 1.9V, 2mA. It showed a gain of 9.5dB with a 2.1dB NF and an IIP3 of –3dBm. The IIP3 was estimated to be 10dB better than would have been obtained from a non-transformer design.

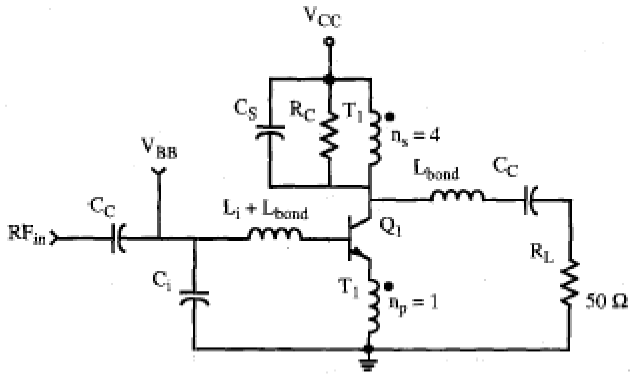

V_{CC}
C_S
R_C
T_1
$n_s = 4$
V_{BB}
L_{bond}
C_C
C_C
$L_i + L_{bond}$
Q_1
RF_{in}
C_i
T_1
$n_p = 1$
R_L
50 Ω

Figure 1.11 – Transformer Feedback Amplifier [9]

The final class of lossless amplifier is the *op-amp* type of amplifier, an example of which is shown in Figure 1.12. In the paper by Nozal [10], the author proposed using series-capacitative feedback to produce a broadband MMIC amplifier built using a PHEMT GaAs process that achieves less than 1.4dB noise figure up to 5GHz and 25dB of gain up to 7GHz, although no mention was made of the amplifier linearity or stability.

The phase of the feedback circuit is controlled with additional resistors in parallel with the feedback capacitors. It is possible to achieve a similar topology with inductive feedback but perhaps with less control and narrower bandwidth. Such a topology with inductive feedback on an IC has not been found in the literature. This is the only published example of this type of amplifier.

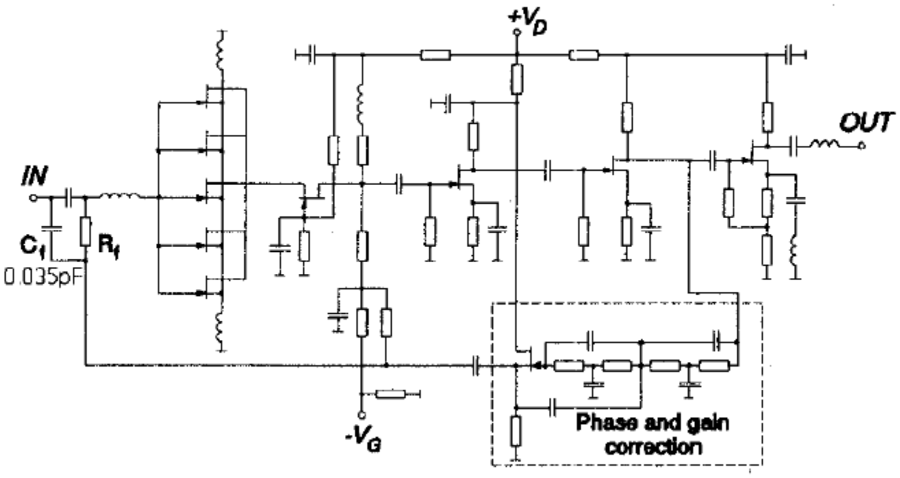


Figure 1.12 – RF Op-Amp lossless feedback amplifier [10]

1.4 Amplifier Performance Considerations

There are several amplifier performance measures that are affected by adding feedback to an amplifier. One of which is amplifier linearity, specifically the third-order-intercept point, but also to a lesser extent the 1dB compression point. Table 1.3 summaries the amplifier factors that are likely to change when feedback is added.

The most obvious advantage to adding feedback around an amplifier is that feedback now controls the gain of that amplifier. This is a useful feature if the amplifier gain is found to vary because of processing variations or with temperature or supply voltage. Adding feedback controls and defines the gain, but of course is subject to tolerances of its own.

If the gain of the amplifier is to be dominated by the feedback components, then the gain of the gain-block needs to be substantially higher, preferably more than 10dB higher than the gain of the required final amplifier design. For example if an amplifier of 10dB gain is required, then the gain-block should have a gain of at least 20dB before feedback is added.

A large motivation for adding feedback to an amplifier is to improve the amplifier linearity, specifically the IIP3. Simulations of an ideal amplifier shown in section 1.4.1, Figure 1.15 shows that the IIP3 increases in proportion to the gain in the gain-block.

A second measure of amplifier linearity, the 1dB compression point is unlikely to change much when feedback is added as this is dominated by the supply voltage and the corresponding output peak-to-peak voltage swing. However a small improvement should be expected as the 1dB compression curve changes from a soft curve to a hard curve with the feedback mechanism keeping the amplifier linear right up to the point when the amplifier output clips.

Linearity	The output signal from an amplifier should ideally be a perfect amplification of the input signal without distortion and harmonics. Feedback improves the amplifier linearity and is the primary motivation for investigating this type of amplifier.
Gain & Bandwidth	Feedback reduces the gain and flattens the bandwidth of the amplifier.
Input & Output Impedances	When feedback is added to an amplifier this will change both input and output impedances. This may be desirable depending on the application. If directional couplers are used in the feedback path then these impedance changes can be minimized.
Circuit Complexity	Feedback makes the circuit more complex and adds cost.
Stability	The amplifier is much more likely to become unstable and produce unwanted oscillations.
Noise Figure	Conventional resistive feedback adds noise to the output and increases the amplifier Noise Figure. Lossless feedback using reactive components should minimize the added noise.

Table 1.3 – Summary of Amplifier factors that change with feedback

The feedback from the RF directional coupler should not contribute to the NF of the amplifier other than with additional forward path losses that need to be kept to a minimum. Some topologies do not use an input coupler, for example the *Transformer-Feedback* amplifier and the *RF-op-amp*, with these the NF should not change but the input and output impedances of these topologies will change more than with those amplifiers that use a directional coupler.

Finally, adding feedback increases the chance of the amplifier being unstable and this will need to be closely watched during the design. There are now two instability loops associated with the amplifier, the normal mechanism around the transistor itself and a second loop when the feedback path is added.

1.4.1 Simulation Results of an Ideal LF Amplifier

A good demonstration of the advantages of lossless-feedback is to simulate an ideal lossless-feedback amplifier shown in Figure 1.13. In this example a lossless coupled line (CLIN) is added to an ideal gain-block (AMP1) that has a variable gain and a NF of 3dB. The gain of the gain-block and the coupling level can be independently controlled.

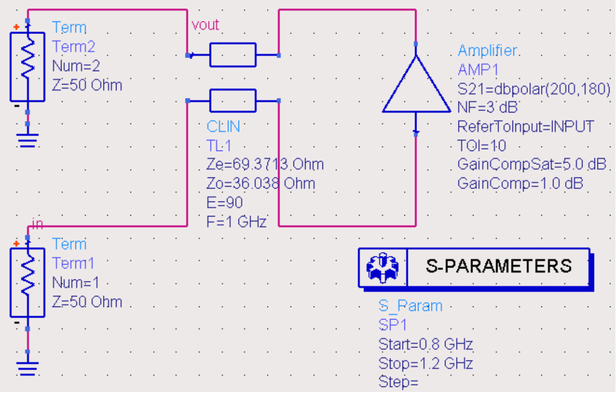


Figure 1.13 – Simulation circuit for an *Ideal* Norton Amplifier

The RF coupler is set to 10dB with Zo = 36.04-Ohm and Ze = 69.37-Ohm; the calculation of Zo and Ze can be found in the MathCAD sheet “Values for Discrete Component Coupler” Appendix A (page 88). The gain-block is an inverting amplifier with its gain adjusted from 5 to 50dB. Unlike a real amplifier there is no variation of phase and gain with frequency.

Figure 1.14 shows how the amplifier gain converges to the value of the coupler, in this case 10dB when the gain in the gain-block is set to a very high level. If the gain of the gain-block is 20dB (10dB above the coupling level), then the amplifier will give 7.9dB gain.

Figure 1.15 shows how the amplifier IIP3 increases as the gain the gain-block increases. If a gain of 50dB can be obtained from the gain-block, then the IIP3 of the amplifier would increase by 60dB, which is a remarkable result. It may be possible to achieve such a large gain using a multiple transistor stage amplifier. At more realistic gain of 20dB, the ideal amplifier shows an improvement of 20dB in the IIP3.

The advantage to the system designer of a high IIP3 can be realized in two ways. It either allows the design of a very robust front-end amplifier that requires little filtering before the mixer, or it allows the power consumption in the amplifier to be reduced considerably and yet still meet the IIP3 requirements imposed by the system design.

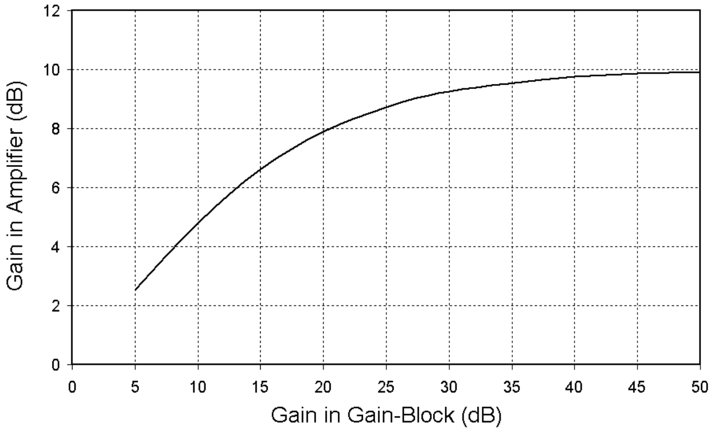


Figure 1.14 – Amplifier Gain Vs Gain-Block Gain With 10dB coupler

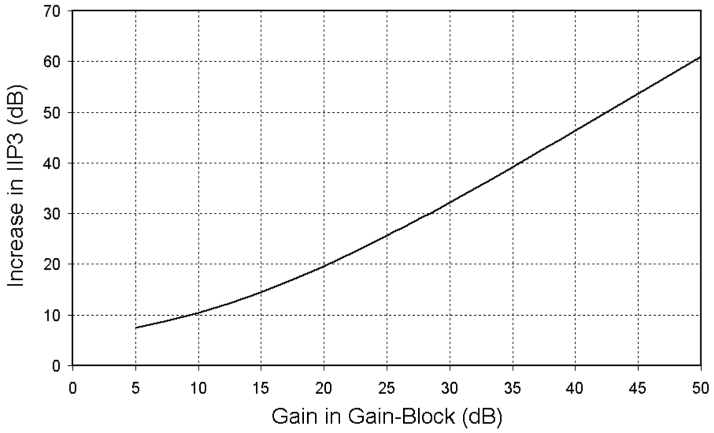


Figure 1.15 – Increase in IIP3 as Gain changes in the Gain-Block With 10dB Coupler

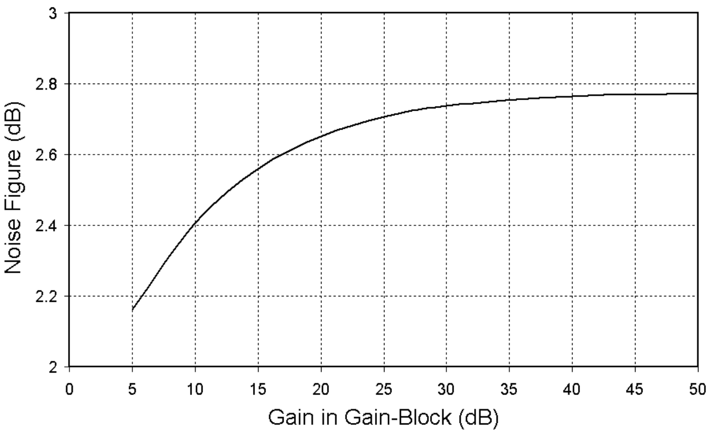


Figure 1.16 – NF Vs Gain-Block Gain With 10dB Coupler

Figure 1.16 shows how the NF of the ideal system varies as the gain in the gain-block changes. Interestingly, the NF of the amplifier is found to be less than the NF of the gain-block. The reason for this is that a percentage of the input power reaches the output directly through the coupler and does not pass through the amplifier.

1.5 Project Goals

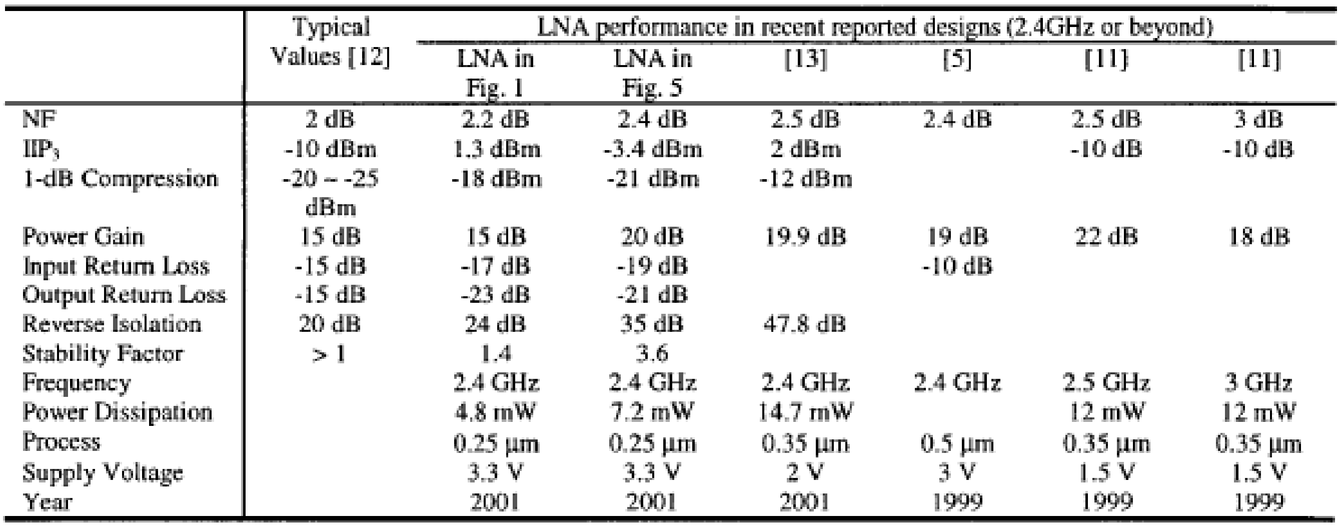
The aim of this project is to investigate and to build a lossless-feedback amplifier on an IC using the UMC-025um RF CMOS process that will demonstrate the principles of this group of amplifiers. The amplifier topology chosen for integration is the topology presented in the original *Norton Amplifier* patent [1] and shown in Figure 1.8. This is the simplest of the lossless feedback amplifiers; it uses a 50-Ohm RF directional coupler as the feedback path and a simple one-transistor amplifier as the gain-block. The coupler is designed and simulated separately to the gain-block. The gain-block is limited in the UMC process to CMOS transistors that are not ideal as gain-block requires 50-ohms input and output termination for optimum performance and the high input impedance of the CMOS transistors may be a challenge to this. However this is suitable choice to demonstrate the principles behind this group of amplifiers.

Chapter 2 describes the design of the Norton Amplifier; Chapters 3 explains layout choices with the final amplifier described in Chapter 4. The test results are presented in Chapter 5.

It is worth considering at this stage, the performance that has been achieved from other LNA designs using a CMOS process, and to use this information as a benchmark to write some design goals. Summaries of LNA performances have been presented in the literature [11] and shown here in Table 1.4. This shows that the typical performance of a CMOS amplifier is a NF=2.5dB, IIP3 = 0dBm, Gain 18dB, Operating voltage 3.3V and 10mW power consumption.

These summaries can be used to create some design goals for the Norton Amplifier design in Chapter 2 and these are listed in Table 1.5.

The input and output impedances are required to be 50-Ohm which is necessary if the amplifier is to be accurately measured and characterized using standard test equipment. The proposed gain is 8dB, which is a compromise as the gain of the amplifiers in table 1.4 are typically 20dB and this will be reduced considerably when feedback is added. The supply voltage is set to 1.25V, this is chosen because the simple Norton amplifier uses a single transistor stage and will thus operate comfortably at this low voltage. In addition this will help the amplifier meet the proposed the power consumption requirement.



	Typical Values [12]	LNA performance in recent reported designs (2.4GHz or beyond)					
		LNA in Fig. 1	LNA in Fig. 5	[13]	[5]	[11]	[11]
NF	2 dB	2.2 dB	2.4 dB	2.5 dB	2.4 dB	2.5 dB	3 dB
IIP_3	-10 dBm	1.3 dBm	-3.4 dBm	2 dBm		-10 dB	-10 dB
1-dB Compression	-20 ~ -25 dBm	-18 dBm	-21 dBm	-12 dBm			
Power Gain	15 dB	15 dB	20 dB	19.9 dB	19 dB	22 dB	18 dB
Input Return Loss	-15 dB	-17 dB	-19 dB		-10 dB		
Output Return Loss	-15 dB	-23 dB	-21 dB				
Reverse Isolation	20 dB	24 dB	35 dB	47.8 dB			
Stability Factor	> 1	1.4	3.6				
Frequency		2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.5 GHz	3 GHz
Power Dissipation		4.8 mW	7.2 mW	14.7 mW		12 mW	12 mW
Process		0.25 µm	0.25 µm	0.35 µm	0.5 µm	0.35 µm	0.35 µm
Supply Voltage		3.3 V	3.3 V	2 V	3 V	1.5 V	1.5 V
Year		2001	2001	2001	1999	1999	1999

Table 1.4 – Summary of CMOS LNA Performance [11]

Linearity	IIP3 = +20dBm
Gain	+8dB
Bandwidth	1.5 to 2GHz,
Input & Output Impedances	50-Ohm with VSWR of 2:1
Stability	Unconditionally Stable.
Noise Figure	3.5dB max. Aim for a NF of less than 3dB, but not thought possible as the coupler is expected to add loss and degrade the NF by 1dB.
Voltage	1.25V
Power	Power dissipation 15mW max.

Table 1.5 – Design Goals for Norton Amplifier

2 NORTON AMPLIFIER DESIGN

2.1 Overall Design Philosophy

This chapter explains the design of the simple Norton lossless-feedback amplifier. The topology of this amplifier is from a solution patented in 1971 [1] by D Norton of the Anzac Corporation and shown in Figure 1.7. In this solution two independent transformers are wound to form a single RF directional coupler [14] that has zero phase-shift between ports P4 and P2. Some of the output power from the transistor at P4 is fed back to its input port P2 at zero-phase, thus creating a feedback path in much the same way as a resistive element could be used.

With this topology, for optimum performance the base and collector impedance of the transistor should be the same as the impedance of the IN and OUT ports. For a 50-Ohm amplifier the base and collector impedances should be 50-Ohm.

The design of this amplifier divides into two parts; design of the RF directional coupler and design of the gain-block. Section 2.2 of this report investigates the properties of a number of RF directional couplers; section 2.3 investigates the different gain-blocks with the complete amplifier, combining the two parts in section 2.4.

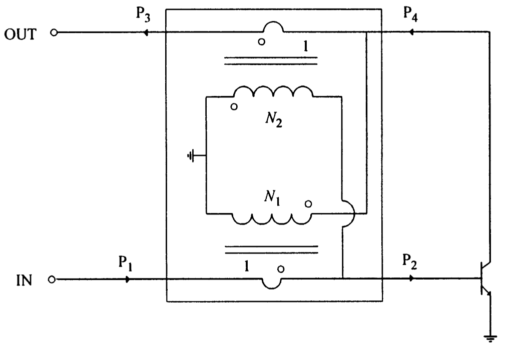


Figure 2.1 – Norton Lossless Feedback Amplifier [6]

2.2 Design of RF Directional Coupler

The RF directional coupler feeds power back from the output of the amplifier to the input, thus forming the feedback path. Ideally the coupler has no loss in the two wanted signal paths, from P1 to P2 and P4 to P3, as this reduces the amplifier gain and adds noise. In addition, the phase-shift through the coupler needs to be well controlled and close to zero degrees as the power feeds back from P4 to P2.

Three coupler options are investigated for suitability, the branch-line coupler, the discrete component transmission line coupler and finally the transformer coupler.

2.2.1 Branchline Coupler

A *Branchline-coupler* is shown in Figure 2.2. This comprises of four transmission lines sections each with a length of 90-degrees and each of defined impedance. The coupler can be designed such that the output powers at Port A and Port B are unequal, with either most of the power outputting at Port A or most at Port B.

Two MathCAD sheets are written that calculate the line impedances for both of these options with different coupling levels. These are be found in Appendix A, pages 86, 87. These sheets start by calculating the required line impedances and then converting this to equivalent discrete components values.

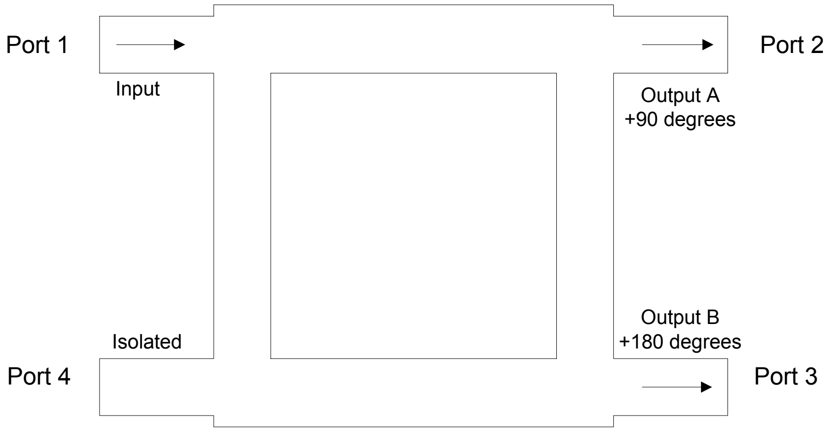
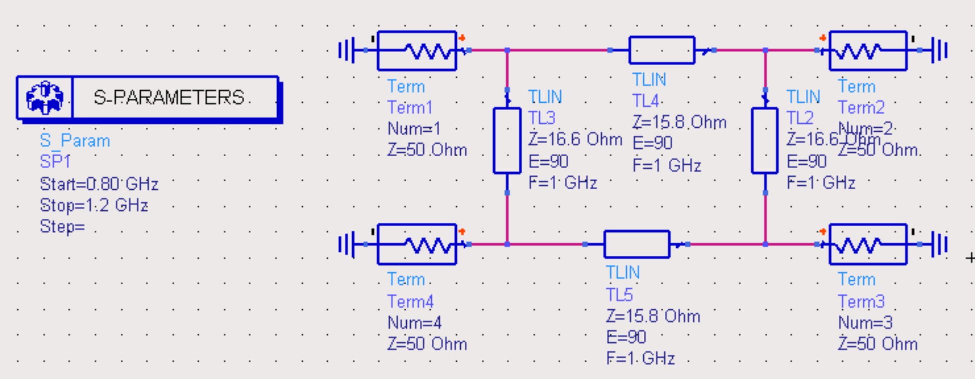


Figure 2.2 – Branchline Coupler

Using the MathCAD design sheet on page 86, an RF coupler can be designed with a coupling factor of 10dB, where most of the input power goes from port 1 to port 3, and has a 10dB coupling from port 1 to 2. Such a coupler is simulated using ADS and shown in Figure 2.3 with the results in Figure 2.4. The losses in the forward path are 0.43dB and the coupling power (S43) is close to -10dB at the operating frequency and with a well-defined phase rotation.



S_Param
SP1
Start=0.80 GHz
Stop=1.2 GHz
Step=

Term
Term1
Num=1
Z=50 Ohm

TLIN
TL3
Z=16.6 Ohm
E=90
F=1 GHz

TLIN
TL4
Z=15.8 Ohm
E=90
F=1 GHz

TLIN
TL2
Z=16.6 Ohm
E=90
F=1 GHz

Term
Term2
Num=2
Z=50 Ohm

Term
Term4
Num=4
Z=50 Ohm

TLIN
TL5
Z=15.8 Ohm
E=90
F=1 GHz

Term
Term3
Num=3
Z=50 Ohm

Figure 2.3 – Branchline Coupler type-1

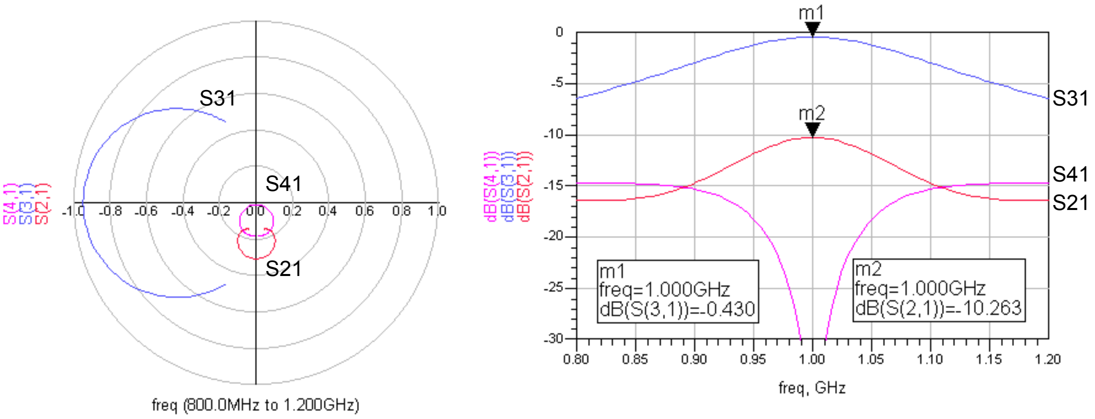


Figure 2.4 – Simulation Results for Branchline Coupler type-1. The forward loss is 0.43dB and the coupled power is –10.26dB and has a well-defined phase rotation.

To use this coupler as part of an amplifier, an additional 90-degree phase rotation needs to be added in the feedback path and the gain-block itself needs to be non-inverting. Such an ideal amplifier is shown in Figure 2.5. The additional phase rotation is added using transmission lines components and these have the further advantage that they can be used to compensate for any unwanted phase shift in the amplifier.

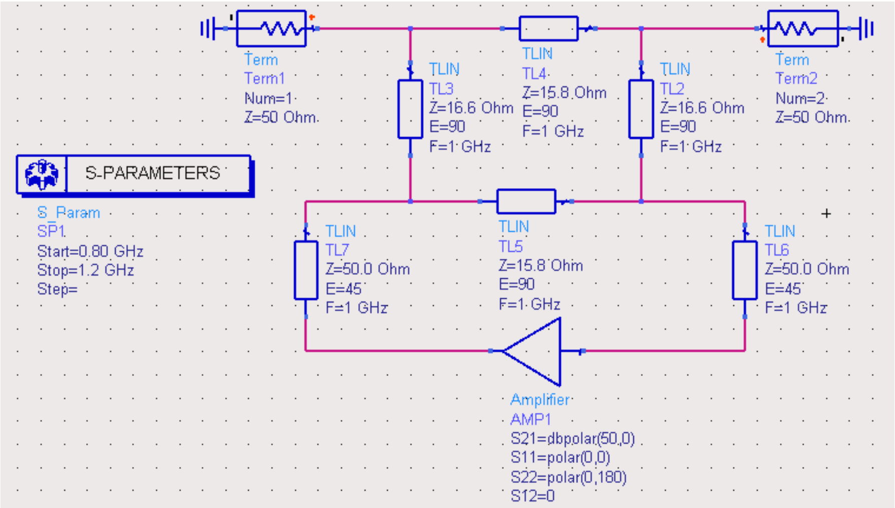

Term
Term1
Num=1
Z=50 Ohm
TLIN
TL3
Z=16.6 Ohm
E=90
F=1 GHz
TLIN
TL4
Z=15.8 Ohm
E=90
F=1 GHz
TLIN
TL2
Z=16.6 Ohm
E=90
F=1 GHz
Term
Term2
Num=2
Z=50 Ohm
S-PARAMETERS
S_Param
SP1
Start=0.80 GHz
Stop=1.2 GHz
Step=
TLIN
TL7
Z=50.0 Ohm
E=45
F=1 GHz
TLIN
TL5
Z=15.8 Ohm
E=90
F=1 GHz
TLIN
TL6
Z=50.0 Ohm
E=45
F=1 GHz
Amplifier
AMP1
S21=dbpolar(50,0)
S11=polar(0,0)
S22=polar(0,180)
S12=0

Figure 2.5 – Amplifier Design using Branchline Coupler type-1

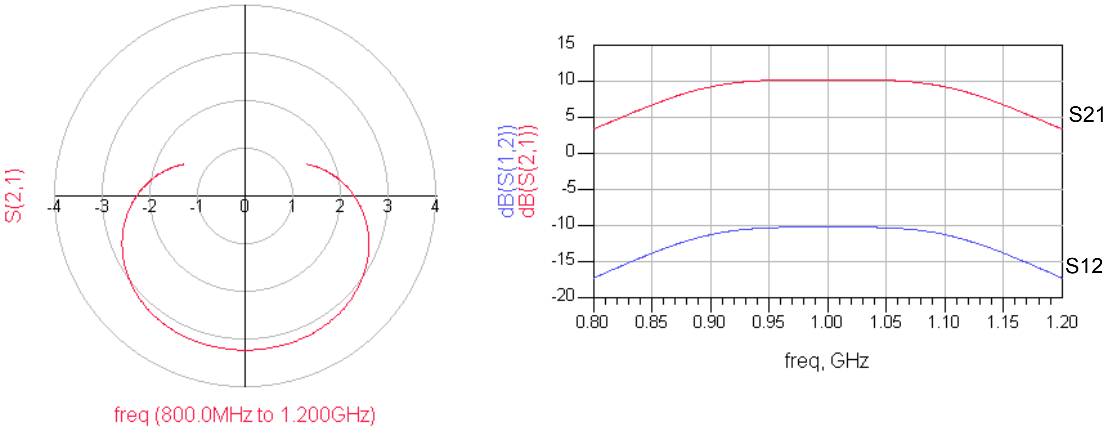


Figure 2.6 – Simulation Results for Branchline Coupler Amplifier type-1

The simulation results for this amplifier are shown in Figure 2.6 and show that an excellent gain and frequency response can be obtained. The gain-block in this simulation is set to 50dB with zero-degrees phase shift rather than a more realistic gain, as it better demonstrates the principles behind this configuration. The reverse isolation is as predicted, equal to the coupling value.

There are a number of alternate variations that may be used with the *Branchline-coupler* that will remove the requirement for this additional phase shifting circuit and will give the amplifier a greater bandwidth. Two alternate topologies are shown in Figures 2.7 and 2.9. The simplest change is to use the alternate coupler design (Figure 2.7) where most of the input power goes from port 1 to port 2 with the -10dB coupling from port 1 to 3. The advantage with this topology is that the feedback path around the amplifier already travels through two 90-degree sections and is therefore at the correct phase for stable feedback without additional circuitry with a non-inverting gain-block.

An amplifier using this coupler variant is shown in Figure 2.7, again with a 50dB gain-block and with the simulation results in 2.8. Surprisingly this amplifier has a wider bandwidth even though the feedback path is also through two 90-degree sections each with a frequency response. The gain and reverse isolation are also 10dB and -10dB, equal to the coupling value.

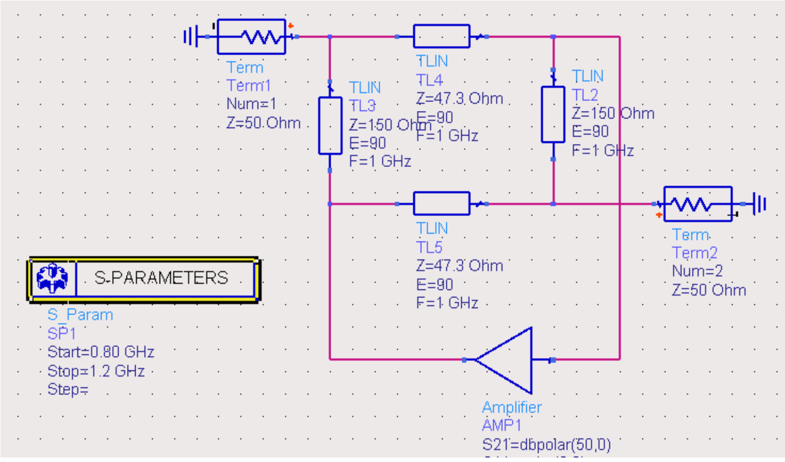

Term
Term1
Num=1
Z=50 Ohm
TLIN
TL3
Z=150 Ohm
E=90
F=1 GHz
TLIN
TL4
Z=47.3 Ohm
E=90
F=1 GHz
TLIN
TL2
Z=150 Ohm
E=90
F=1 GHz
TLIN
TL5
Z=47.3 Ohm
E=90
F=1 GHz
Term
Term2
Num=2
Z=50 Ohm
S-PARAMETERS
S_Param
SP1
Start=0.80 GHz
Stop=1.2 GHz
Step=
Amplifier
AMP1
S21=dbpolar(50,0)

Figure 2.7 – Branchline Coupler Amplifier type-2

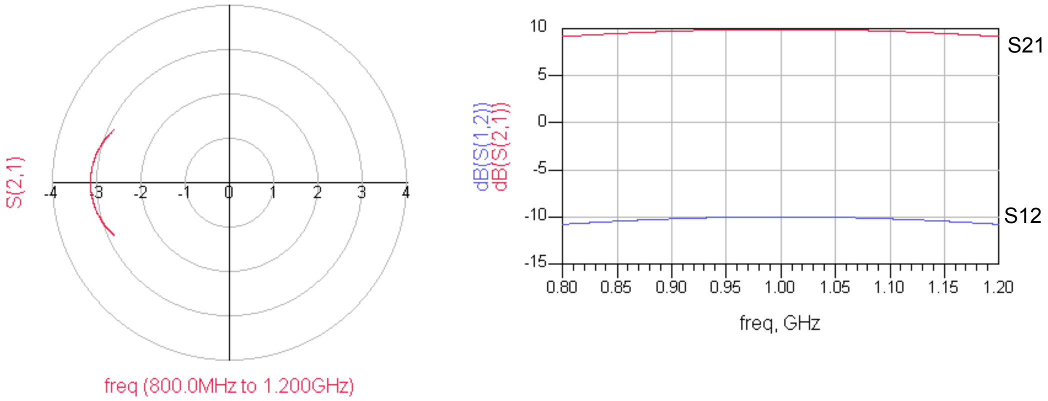


Figure 2.8 - Simulation Results for Branchline Coupler Amplifier type-2

The final improvement is to consider the use of a multiple section Branchline coupler that will increase the bandwidth and also remove the requirement for additional phase shifting. A circuit showing a 3dB amplifier with a two section Branchline coupler is shown in Figure 2.9. The simulation results show a bandwidth of 0.5 to 1.5GHz, the amplifier shows excellent results.

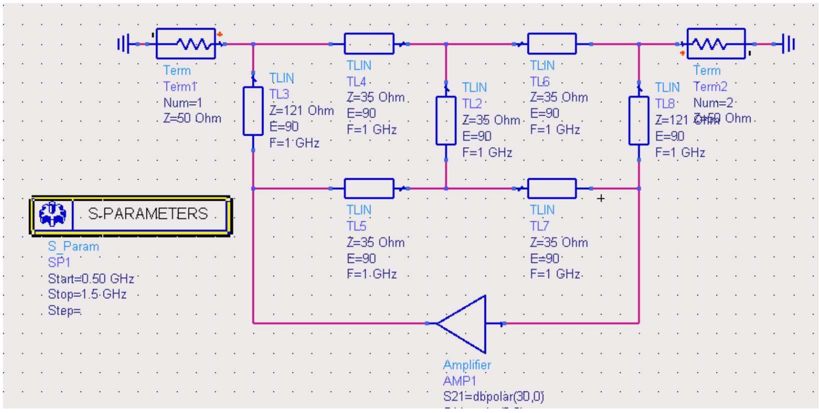

Term
Term1
Num=1
Z=50 Ohm
TLIN
TL3
Z=121 Ohm
E=90
F=1 GHz
TLIN
TL4
Z=35 Ohm
E=90
F=1 GHz
TLIN
TL2
Z=35 Ohm
E=90
F=1 GHz
TLIN
TL6
Z=35 Ohm
E=90
F=1 GHz
TLIN
TL8
Z=121 Ohm
E=90
F=1 GHz
Term
Term2
Num=2
Z=50 Ohm
TLIN
TL5
Z=35 Ohm
E=90
F=1 GHz
TLIN
TL7
Z=35 Ohm
E=90
F=1 GHz
S-PARAMETERS
S_Param
SP1
Start=0.50 GHz
Stop=1.5 GHz
Step=
Amplifier
AMP1
S21=dbpolar(30,0)

Figure 2.9 - Branchline Coupler Amplifier type-3

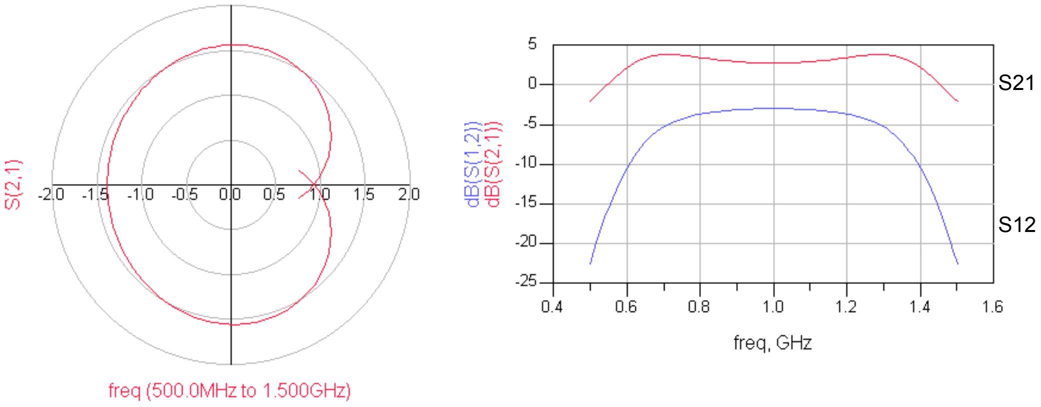


Figure 2.10 - Simulation Results for Branchline Coupler Amplifier type-3

2.2.1.1 Branchline Coupler on the IC

The Branchline coupler seems to shows promise as a coupler that could be used in the design of a lossless-feedback amplifier, but before moving into a detailed design phase a more realistic coupler needs to be simulated with losses included. To estimate the expected losses, each of the 90-degree sections can be translated into a C-L-C transmission line. This is essential for integration, as a 90-degree transmission line is several centimeters long at 2GHz and is impractical on an IC.

For the Branchline Coupler shown in Figure 2.3, at 2GHz for a –12dB coupling, the inductance values are 1nH and the capacitance is 12.5pF. The equivalent series resistance for this inductor is estimated by comparing the UMC model [15] for the standard 1nH square inductor. The Q of the UMC inductor is 4 at 1.8GHz, which corresponds to an equivalent series resistance of 2.8-Ohm. These simulations are made with a lower value than this at 2-Ohm as it is expected that using wider tracks will reduce the losses. The schematic with these series resistors is shown in Figure 2.11 and with the results in Figure 2.12.

The results shows a large deviation from the ideal coupler (Figure 2.4) that renders this topology unacceptable for integration on an IC and unlikely to give acceptable results when used as part of a lossless feedback amplifier. The losses in the transmission paths (S21 & S34) are 3.3dB and the coupling level has dropped by over 4dB to -14.3dB.

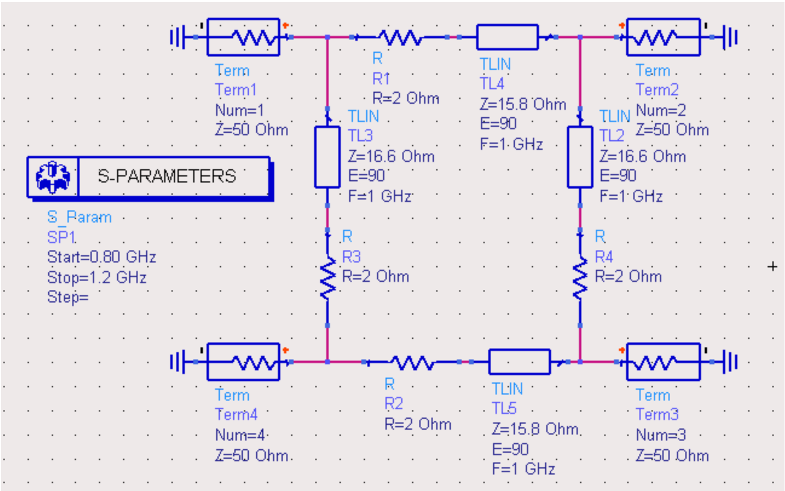

Term
Term1
Num=1
Z=50 Ohm
R
R1
R=2 Ohm
TLIN
TL4
Z=15.8 Ohm
E=90
F=1 GHz
Term
Term2
Num=2
Z=50 Ohm
TLIN
TL3
Z=16.6 Ohm
E=90
F=1 GHz
TLIN
TL2
Z=16.6 Ohm
E=90
F=1 GHz
S-PARAMETERS
S_Param
SP1
Start=0.80 GHz
Stop=1.2 GHz
Step=
R
R3
R=2 Ohm
R
R4
R=2 Ohm
Term
Term4
Num=4
Z=50 Ohm
R
R2
R=2 Ohm
TLIN
TL5
Z=15.8 Ohm
E=90
F=1 GHz
Term
Term3
Num=3
Z=50 Ohm

Figure 2.11 - Branchline Coupler type-1 with Series Resistance

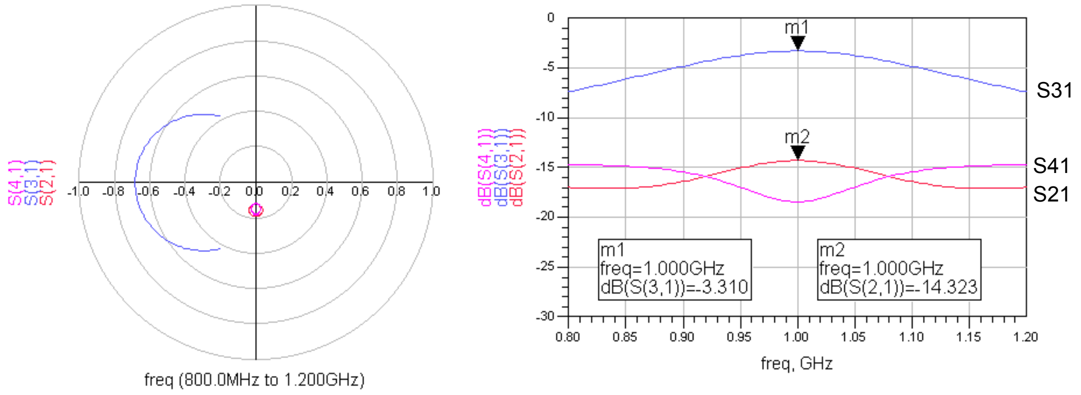


Figure 2.12 – Simulation Results for Branchline Coupler type-1 with Series Resistance

Some consideration was given to using the alternative coupler configuration shown in Figure 2.7, but with a line impedance of 150-Ohm required in this design which correspond to an inductance of 15nH, this would be difficult to achieve and will result in a large coupler.

2.2.2 Transmission Line Coupler

The second option for an RF directional coupler and perhaps the most obvious starting point, is the simple transmission line coupler shown as in Figure 2.13 and this was used in the simulations to demonstrate the principles behind this group of amplifiers in Section 1.4.1.

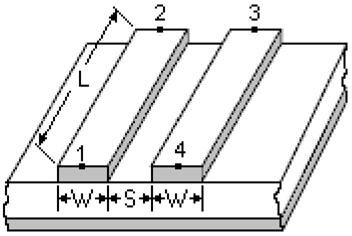


Figure 2.13 – Microstrip Coupled Line

A 10dB coupler is obtained with Zo = 36.04-Ohm and Ze = 69.37-Ohm. Using the line impedance calculator *LineCalc* in *HP ADS* and with the dimensions for H, T and Er from the UMC process [16], this corresponds to a line length of 22mm at 2GHz. This length is clearly unacceptable for integration on an IC, although Ozazaki [21] has produced a coupler of this type with an overall area of 0.9mm by 0.12mm and operates from 10 to 17GHz by meandering the Microstrip tracks on a GaAs substrate.

To achieve the size constraint it is necessary is to build the coupler using discrete components. The design equations for this are shown in the MathCAD sheet on page 88, with the formulas taken from an IEEE MTT paper by Hogerheiden J [17], and shown diagrammatically in Figure 2.15.

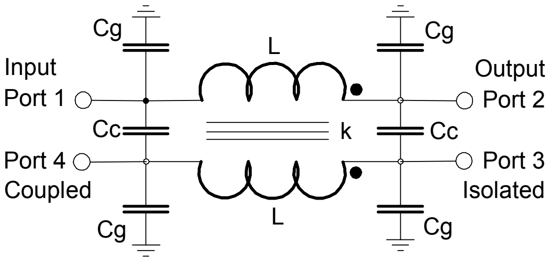


Figure 2.15 – Discrete Component Coupler

A suitable 10dB coupler at 1GHz is shown in Figures 2.16, and the results for the ideal lossless coupler are presented in Figure 2.17. It can be seen that the gain and phase response of S41 is excellent, giving very close to 10dB coupling at the center of the band and with a wider bandwidth than that obtained from the *Branchline-coupler*. Other aspects of the coupler are also good, the forward path loss is 0.47dB and the coupler shows greater than 25dB of isolation (S31) over a wide bandwidth.

Before moving further into the design it is worth taking time to run a simulation with practical losses that will be experienced if this design is integrated on an IC. The equivalent series resistance is estimated from UMC model [15] for an 8nH square inductor, where the Q of this inductor is given as 6 at 1.8GHz. This corresponds to a series resistance of 15-Ohms, but as before it is expected that a practical implementation with wider tracks will produce lower series resistance of 10-Ohms for L2 and 15-Ohms for L1. The difference in the resistance for L1 compared to L2 is because one of the inductor tracks will be on the metal-5 layer that is 2µm thick and the other inductor will be on metal-4 that is 0.6µm thick.

The simulation results are shown in Figure 2.18. This lossy coupler is still reasonable with good phase rotation in the S41 path. The S41 coupling is 11dB and the forward path loss is 2dB.

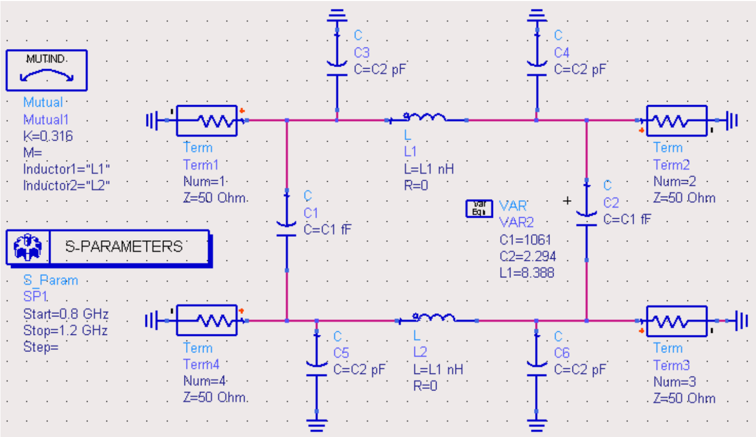

MUTIND
Mutual
Mutual1
K=0.316
M=
Inductor1="L1"
Inductor2="L2"
S-PARAMETERS
S_Param
SP1
Start=0.8 GHz
Stop=1.2 GHz
Step=
C
C3
C=C2 pF
C
C4
C=C2 pF
Term
Term1
Num=1
Z=50 Ohm
L
L1
L=L1 nH
R=0
Term
Term2
Num=2
Z=50 Ohm
C
C1
C=C1 fF
VAR
VAR2
C1=1061
C2=2.294
L1=8.388
C
C2
C=C1 fF
Term
Term4
Num=4
Z=50 Ohm
C
C5
C=C2 pF
L
L2
L=L1 nH
R=0
C
C6
C=C2 pF
Term
Term3
Num=3
Z=50 Ohm

Figure 2.16 – 1GHz 10dB Discrete Component Coupler

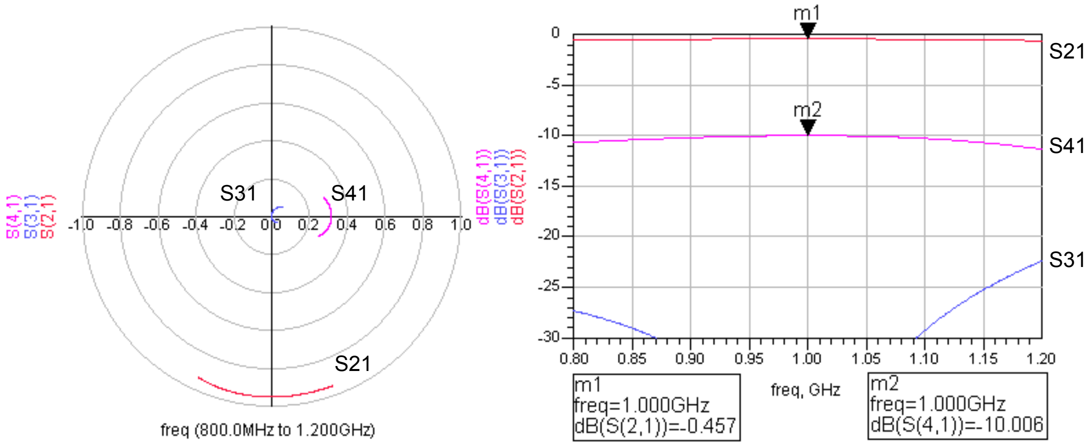


Figure 2.17 – Simulation Results for 1GHz 10dB Discrete Component Coupler Without losses

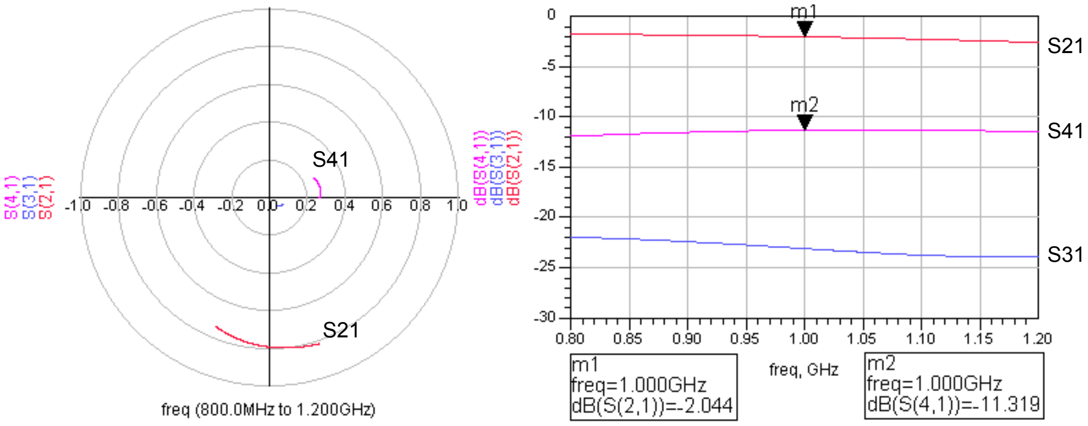


Figure 2.18 – Simulation Results for 1GHz 10dB Discrete Component Coupler With Losses (L1 with 10R; L2 with 15R)

A disadvantage of this topology is that the coupler needs to be designed with a small amount of mutual coupling between the turns that may be hard to achieve and it is worth investigating an alternative coupler configuration shown in Figure 2.19 [22] that uses four inductors but does not require mutual coupling between them.

Simulations have shown that this circuit works well with less than –15dB of coupling, but at higher coupling levels the phase rotation and coupling levels are not well defined. Results for the coupler at 1GHz and at 10dB and 20dB coupling are shown in Figures 2.20 and 2.21. These show a poor performance at 10dB but good performance at 20dB.

Apart from the poor phase response at higher coupling levels, the circuit has twice the number of inductors which will consume approximately four times the IC area of the coupled inductor version. In addition the circuit has approximately twice the path loss compared to the coupled version.

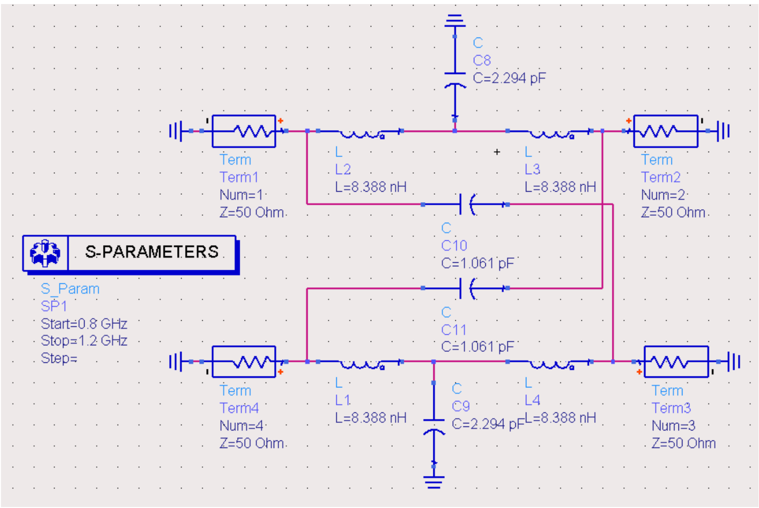

C
C8
C=2.294 pF
Term
Term1
Num=1
Z=50 Ohm
L
L2
L=8.388 nH
L
L3
L=8.388 nH
Term
Term2
Num=2
Z=50 Ohm
S-PARAMETERS
S_Param
SP1
Start=0.8 GHz
Stop=1.2 GHz
Step=
C
C10
C=1.061 pF
C
C11
C=1.061 pF
Term
Term4
Num=4
Z=50 Ohm
L
L1
L=8.388 nH
C
C9
C=2.294 pF
L
L4
L=8.388 nH
Term
Term3
Num=3
Z=50 Ohm

Figure 2.19 – 1GHz 10dB Discrete Component Coupler type 2

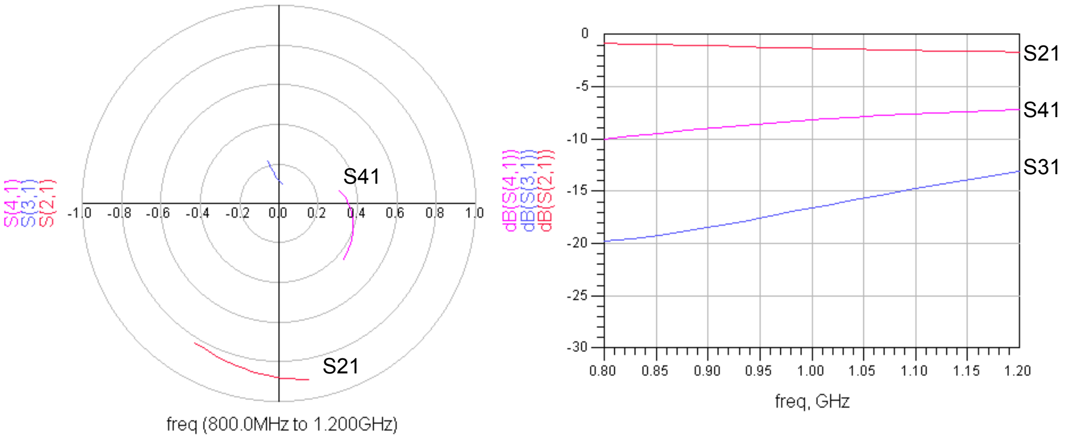


Figure 2.20 – Simulation Results for 10dB Discrete Component Coupler type 2

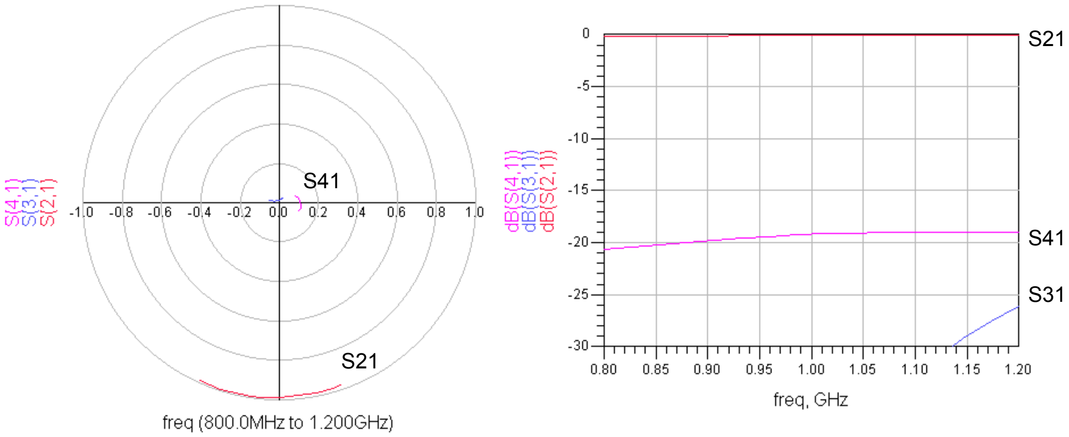


Figure 2.21 – Simulation Results for 20dB Discrete Component Coupler type 2

2.2.3 Transformer Coupler

The third coupler option investigated is the transformer coupler as used in the original *Norton Amplifier* patent, with the design equations described in a paper by Kajfez [14]. These equations are presented using the MathCAD sheet on page 93 and show that a turns ration of 3.5:1 is a suitable starting point for the design that will give approximately 11dB of coupling under ideal conditions.

No reference can be found of a coupler of this type having been built on an IC before and this paper implies that a tight coupling (k) of better than 0.99 is required to get good performance at these frequencies. Normally the best coupling (k) that can be achieved using the planar spiral transformers is 0.9 [28] with k = 0.8 considered more likely.

To test this, a simulation circuit is constructed shown in Figure 2.22 that has a value of k = 0.8 and with a primary inductance value of 1.65nH; both of which are considered achievable. The inductance value is proportional to the square of the number of turns, so with a turns-ratio of 3.5 and with 1.65nH primary inductance, the inductance value of the secondary turns is estimated to be 20.21nH with 20nH used in the simulation.

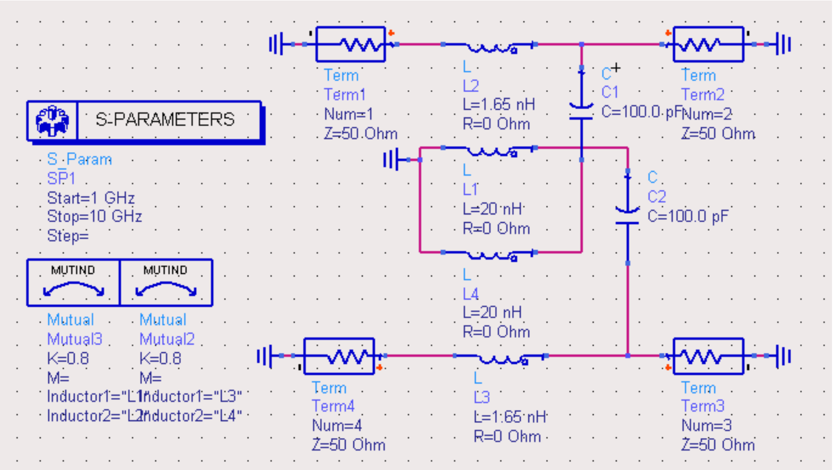

S-PARAMETERS
S_Param
SP1
Start=1 GHz
Stop=10 GHz
Step=
MUTIND
MUTIND
Mutual
Mutual3
K=0.8
M=
Inductor1="L1"
Inductor2="L2"
Mutual
Mutual2
K=0.8
M=
Inductor1="L3"
Inductor2="L4"
Term
Term1
Num=1
Z=50 Ohm
L
L2
L=1.65 nH
R=0 Ohm
C
C1
C=100.0 pF
Term
Term2
Num=2
Z=50 Ohm
L
L1
L=20 nH
R=0 Ohm
C
C2
C=100.0 pF
L
L4
L=20 nH
R=0 Ohm
Term
Term4
Num=4
Z=50 Ohm
L
L3
L=1.65 nH
R=0 Ohm
Term
Term3
Num=3
Z=50 Ohm

Figure 2.22 – 1GHz Transformer Coupler without Losses

The results are shown in Figure 2.23 and it is important to notice that these results are presented over a much wider bandwidth than with the previous coupler designs. The forward path loss (S21) is 0.38dB at 3GHz, and there is a small variation of this up to 10GHz. The coupling (S23) is reasonably flat and has a stable close-to-zero phase shift over this band. The isolation (S31) is excellent.

Interestingly, it can be seen that the coupler is not symmetrical and if reversed such that S41 is the feedback path, it can be seen that there will be a 180-degree phase shift, which will allow a non-inverting amplifier to be used as the gain stage.

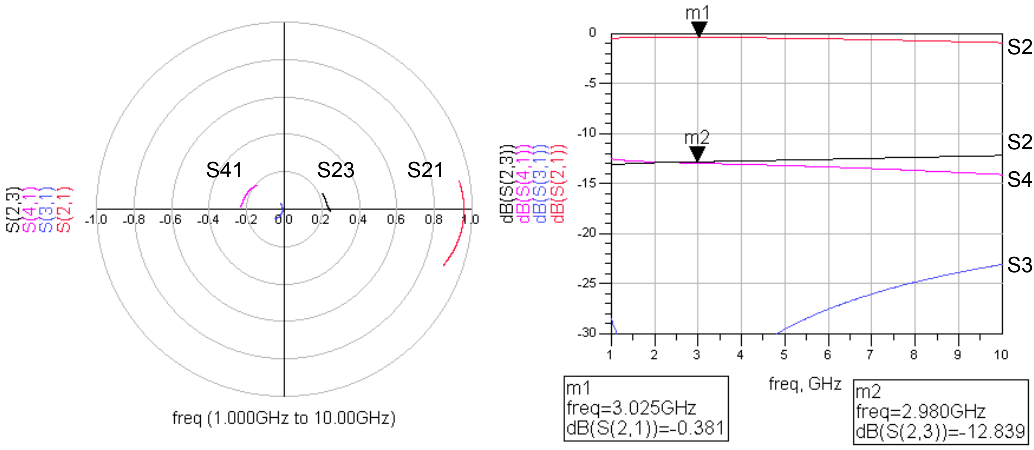


Figure 2.23 – Simulation Results for Transformer Coupler without losses

To check the suitability of this coupler for integration on an IC we need to carry out further simulations with resistive losses; a 2-Ohm series resistance is added to1.6nH inductors and 20-Ohms to the 20nH inductors. The simulation results shown in Figure 2.24 indicate that this circuit is a robust solution with the forward path loss increasing by 0.3dB. Perhaps the only concern is the coupling (S23) that now has a slope over the frequency band.

A simple solution was found to flatten the coupling level over this bandwidth by reducing the decoupling capacitors C1 and C2 from 100pF to something smaller. This of course is advantageous in integrating this design on an IC as the smaller capacitors take up less space. The circuit is simulated with the capacitors set to 6pF and the results shown in Figure 2.25.

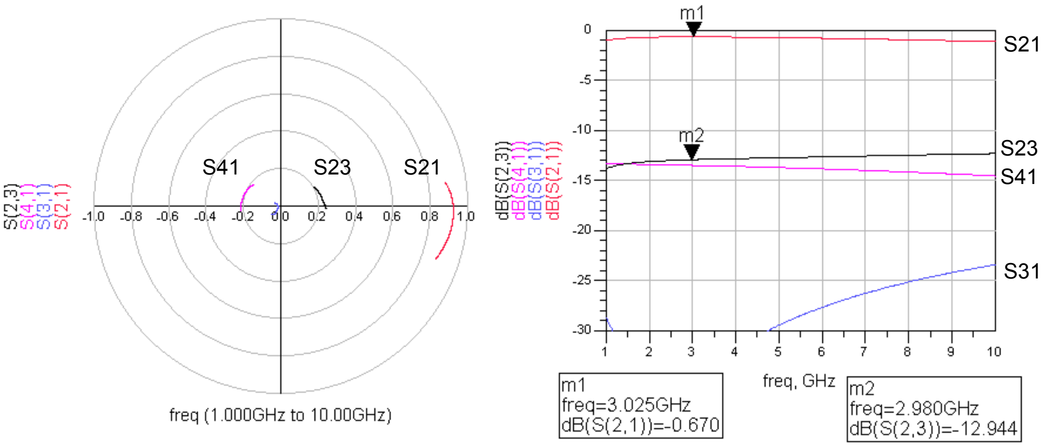


Figure 2.24 – Simulation Results for Transformer Coupler with Losses

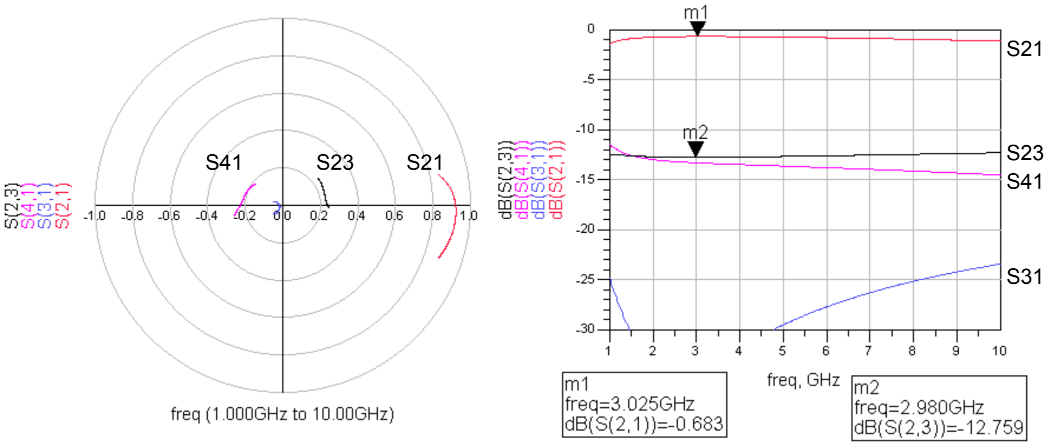


Figure 2.25 –Transformer Coupler with 6pF Decoupling Capacitors

2.2.4 Conclusion on Coupler Options

Three types of coupler have been investigated in this section. The *branch-line* coupler was found to be too sensitive to the expected losses associated with integration and for this reason cannot be used as part of the lossless feedback amplifier. The discrete component transmission line coupler shows several advantages, it is small, requiring two overlapping inductors and with an easily achievable coupling coefficient. The disadvantage is that it is not symmetrical with the construction requiring two different metal layers, each with different conductivity. Nevertheless its small size and good bandwidth gives it advantages. The third coupler investigated is the transformer coupler. This has the widest bandwidth of the couplers investigated, but runs the risk that the high coupling level required is unachievable.

The coupler chosen for integration with the gain-block to form part of the Norton Amplifier is the discrete component coupler. The input path will be on the top metal layer with the highest conductivity to minimize the input loss and the affect on the Noise Figure. Both the discrete component coupler and the transformer coupler are built and tested individually and the results presented in Section 5.

2.3 Design of Gain-Block

2.3.1 Single FET Gain-Block

The simplest gain block that can be built is with a single FET stage, and it is this topology but with a bipolar transistor that was presented in the original Norton amplifier patent. A simulation of the simple FET stage is set up in Figure 2.26 and the results shown in Figure 2.27. The amplifier is not matched, as we will see later that the matching circuits will result in an unwanted phase delay.

The circuit takes 15mA and has a forward path gain of 13dB at 2GHz. This is too low to be useful with 20dB gain considered the minimum for the circuit to be useful, the Noise Figure however is good at 1.8dB, but the stability measures show that this amplifier is likely to be unstable. From this simple construction we can see that a simple transistor amplifier will not work, it does not have sufficient gain and has a tendency to be unstable and consequently it is necessary to consider a multiple transistor amplifier solution.

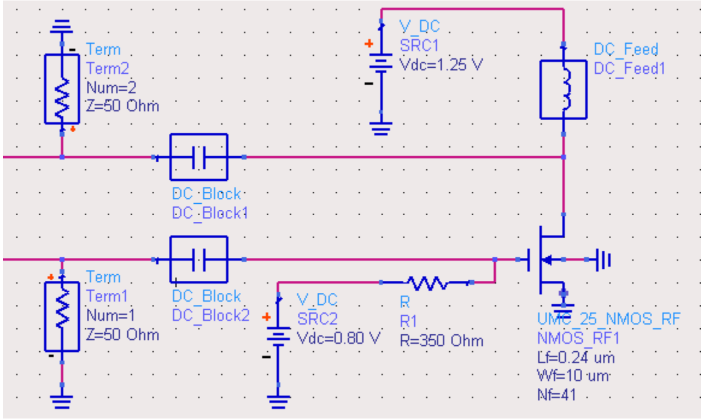

Term
Term2
Num=2
Z=50 Ohm
V_DC
SRC1
Vdc=1.25 V
DC_Feed
DC_Feed1
DC_Block
DC_Block1
Term
Term1
Num=1
Z=50 Ohm
DC_Block
DC_Block2
V_DC
SRC2
Vdc=0.80 V
R
R1
R=350 Ohm
UMC_25_NMOS_RF
NMOS_RF1
Lf=0.24 um
Wf=10 um
Nf=41

Figure 2.26 – Single FET Amplifier Gain Block. Gate length 0.24µm and Gate width 41 x 10µm.

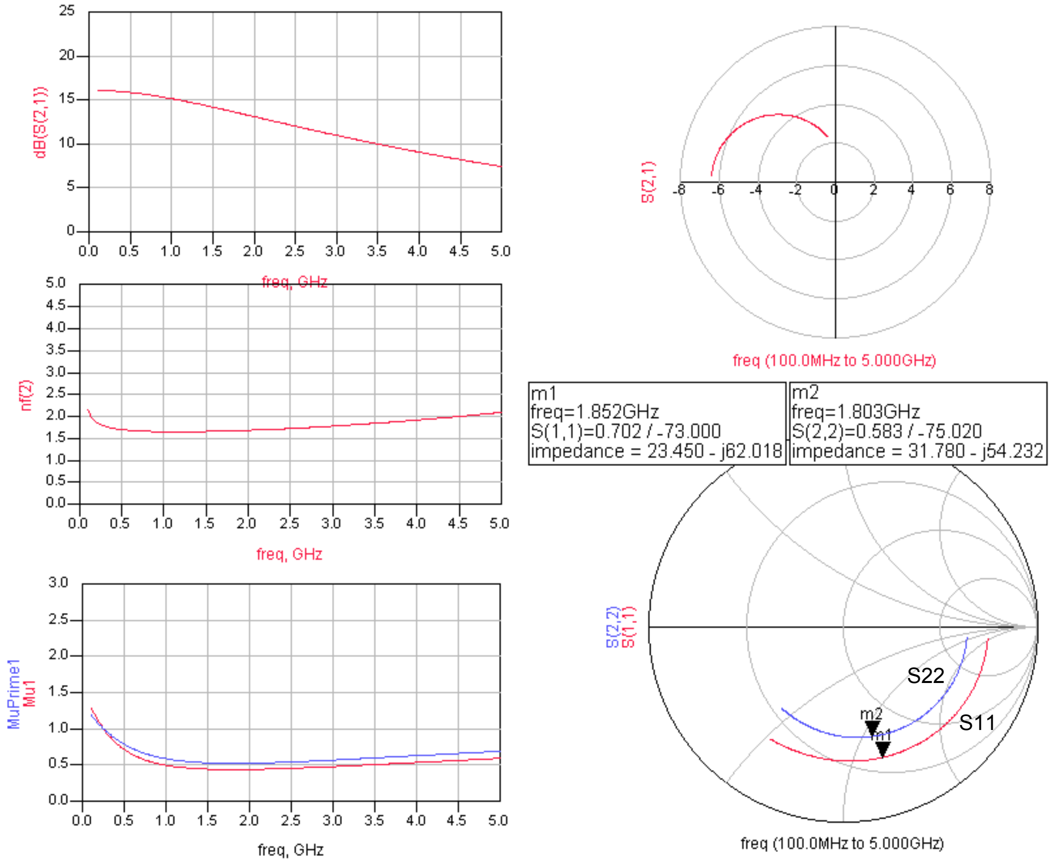


Figure 2.27 – Performance of Single FET Amplifier Gain Block

2.3.2 Multiple Transistor Gain-Block

The logical step from a single FET amplifier is to consider a multiple transistor amplifier such as the amplifier shown in Figure 2.28. In this design a common-gate input configuration was chosen to present a good 50-Ohm input match over a wide bandwidth and this was followed by a cascode FET configuration for high gain. The results of this amplifier are shown in Figure 2.29, the gain has increased to a satisfactory 27dB at 1.8GHz; the NF is worse at 3dB; the stability has improved greatly and the input impedance is closer to 50-Ohms, as expected.

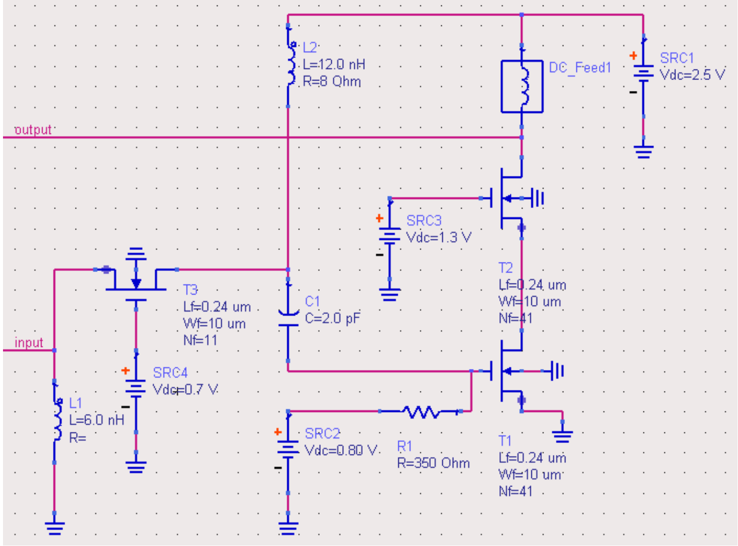

L2
L=12.0 nH
R=8 Ohm
DC_Feed1
SRC1
Vdc=2.5 V
output
SRC3
Vdc=1.3 V
T2
Lf=0.24 um
Wf=10 um
Nf=41
T3
Lf=0.24 um
Wf=10 um
Nf=11
C1
C=2.0 pF
input
SRC4
Vdc=0.7 V
L1
L=6.0 nH
R=
SRC2
Vdc=0.80 V
R1
R=350 Ohm
T1
Lf=0.24 um
Wf=10 um
Nf=41

Figure 2.28 – Multiple Transistor Amplifier

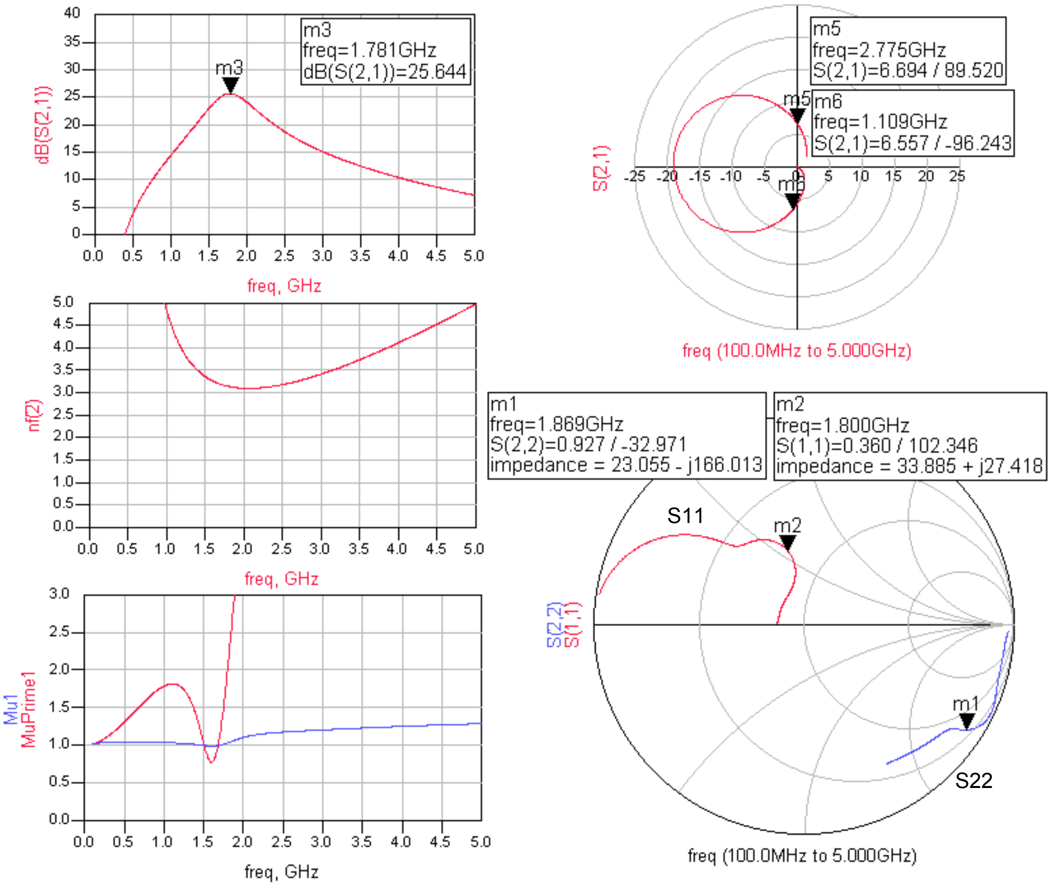


Figure 2.29 - Performance of Complex Gain Block

Generally this amplifier looks like a reasonable candidate for integration as part of an LFA and to test this, the amplifier is added to a 10dB transformer-type coupler of the topology shown in Figure 2.22. The results of the complete amplifier are shown in Figure 2.30 and this is the first time in this report that a realistic lossless feedback amplifier is constructed and analyzed.

There are a number of interesting observations that can be made about this LFA. Firstly, the forward gain (S21) is close to the 10dB expected and is flat across a wide bandwidth. Secondly, the input and output impedance are both closer to 50-Ohms and of an impedance that is better than the gain block. It is interesting that with this type of amplifier both the input and output impedances tend to improve.

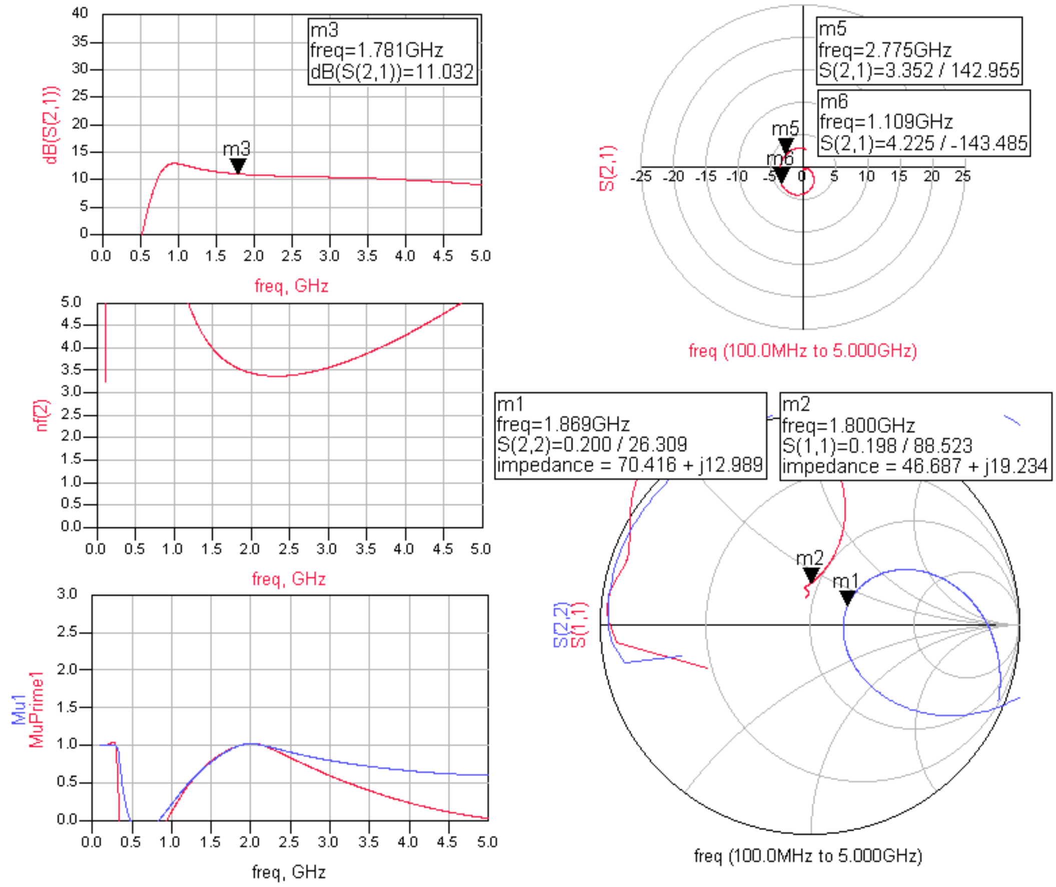


Figure 2.30 - Performance of LFB Amplifier with Complex Gain Block from Figure 2.28 combined with wide bandwidth RF directional Coupler from Figure 2.22

The worst performance change is the stability index as calculated by μ and μ' which now go well below 1, the value required for unconditional stability. At some frequencies *both* stability indices are less than 0, which indicates that the amplifier will be unstable when connected to 50-ohm. The reason for this worsening of stability can be explained by examining the S21 polar plot of the basic amplifier, shown in Figure 2.29.

Normally the output of the amplifier is inverting as seen by the polar plot cutting the x-axis on the left. Unfortunately, the phase of the amplifier output signal becomes positive at below 1.1GHz and above 2.8GHz and this is shown in Figure 2.29 with markers where the response cuts the y-axis. It is important to note that using a gain-block that gives gain with a positive phase is likely to cause the amplifier to be unstable.

The conclusion from this, is that a multi-stage amplifier circuit is unlikely to be usable as it is likely that the phase of S21 changes too much with frequency and will have gain with a non-inverting phase at some point in the frequency response. It is essential that the gain block is as simple as possible.

2.3.3 Two FET Gain-Block

The solution proposed is a two FET gain-block that uses a common source input FET to provide gain, followed by a second FET as a source-follower to improve the output current drive and lower the output impedance closer to 50-Ohm. The circuit is shown in Figure 2.31. The source-follower also provides gain with the advantage that it has little effect on the phase delay. It also provides reverse isolation, which should allow easier integration of the amplifier with the coupler.

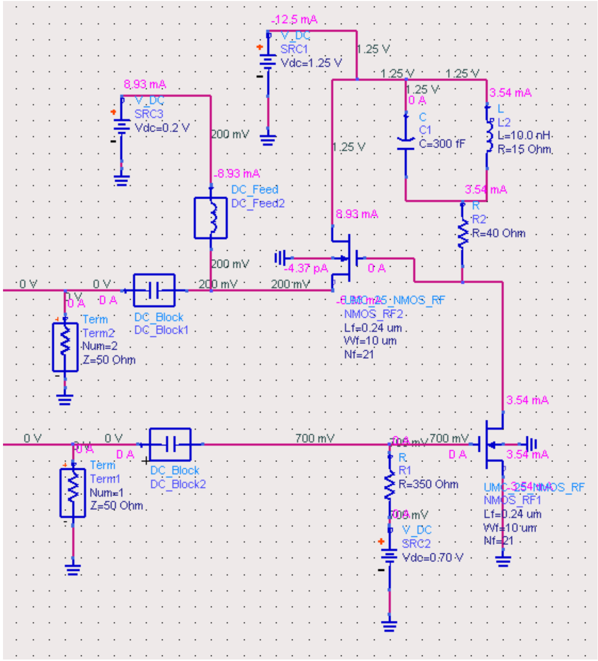

V_DC
SRC1
Vdc=1.25 V
V_DC
SRC3
Vdc=0.2 V
DC_Feed
DC_Feed2
C
C1
C=300 fF
L
L2
L=10.0 nH
R=15 Ohm
R
R2
R=40 Ohm
NMOS_RF
NMOS_RF2
Lf=0.24 um
Wf=10 um
Nf=21
Term
Term2
Num=2
Z=50 Ohm
DC_Block
DC_Block1
Term
Term1
Num=1
Z=50 Ohm
DC_Block
DC_Block2
R
R1
R=350 Ohm
V_DC
SRC2
Vdc=0.70 V
NMOS_RF
NMOS_RF1
Lf=0.24 um
Wf=10 um
Nf=21

Figure 2.31 – Two FET Gain Block

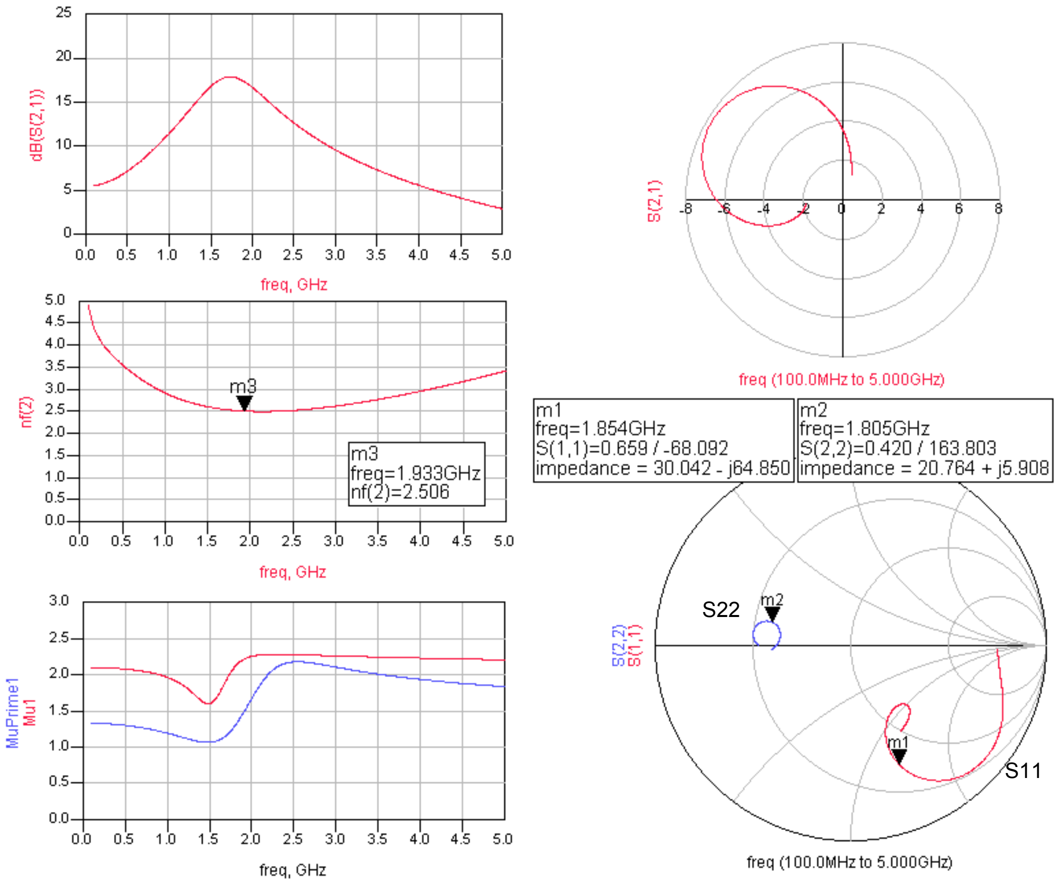


Figure 2.32 – Performance of Two FET Gain Block

The results for this gain-block can be seen in Figure 2.32. The forward gain peaks at 18dB, the NF has a minimum of 2.5dB and it is unconditionally stable. The S21 phase rotation is acceptable, with approximately 20° of phase error and the output impedance is 17-ohms and close to the real axis. These are reasonable results.

It is also worth pointing out that this amplifier is designed for 1.25V operation, as there is little advantage to operating the amplifier at a higher supply voltage. The simple amplifier construction makes it easy to operate at such a low voltage and this minimizes the power consumption.

2.3.4 Addition of Noise Optimization Inductor

The two-FET gain-block shown in the previous section is a reasonable solution that can be combined with a coupler to build a lossless-feedback amplifier. The major concern is the noise figure, which at 3dB is on the high side and will become higher when the coupler losses are included.

One option to reduce the noise figure is to consider adding a tuned circuit in series with the gate-source capacitance and in so doing increasing the Vgs voltage swing, and thereby reducing the noise figure and increasing the gain of the amplifier. The technique for doing this is outlined in this paper [18] and involves measuring the gate-source input capacitance and tuning this out with series inductors. The Cgs of the transistor is measured using the simulator, under the required operating conditions to be 1.28pF. For a tuned circuit to be included then the following equation can be used to calculate the series inductance.

$$Ls + Lg = \frac{1}{(2 \cdot \pi \cdot Frequency)^2 C_{gs}}$$

This gives a total inductance value of 6nH at 1.8GHz; this is divided into two with half placed in series with the *source* and half in series with the *gate* with the ratio of inductors to obtain a 50-Ohm input match. The final circuit is shown in Figure 2.33. An additional advantage of these inductors is the input impedance becomes closer to 50-Ohm and more real.

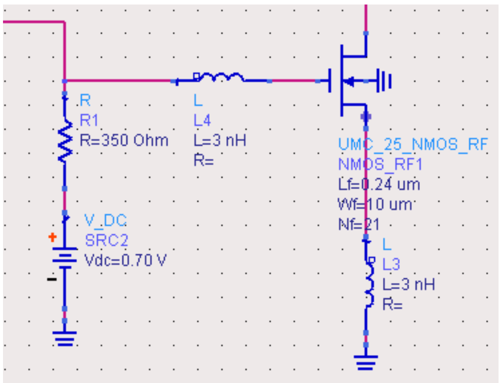


Figure 2.33 – Two FET Gain-Block with Cgs Tuning Inductors

The results presented in Figure 2.34 show an improved Noise Figure to 2.2dB and an improved input match (S11) closer to 50-Ohm. The concern with this modification is the polar response of S21 has rotated clockwise and with now a substantial part of the frequency response with a positive phase shift. This phase shift will cause this circuit to be unstable when combined with an RF directional coupler.

This reinforces the previous lesson that the amplifier must be of minimum complexity to reduce the phase shift in the S21 forward gain to ensure the lossless feedback amplifier remains stable.

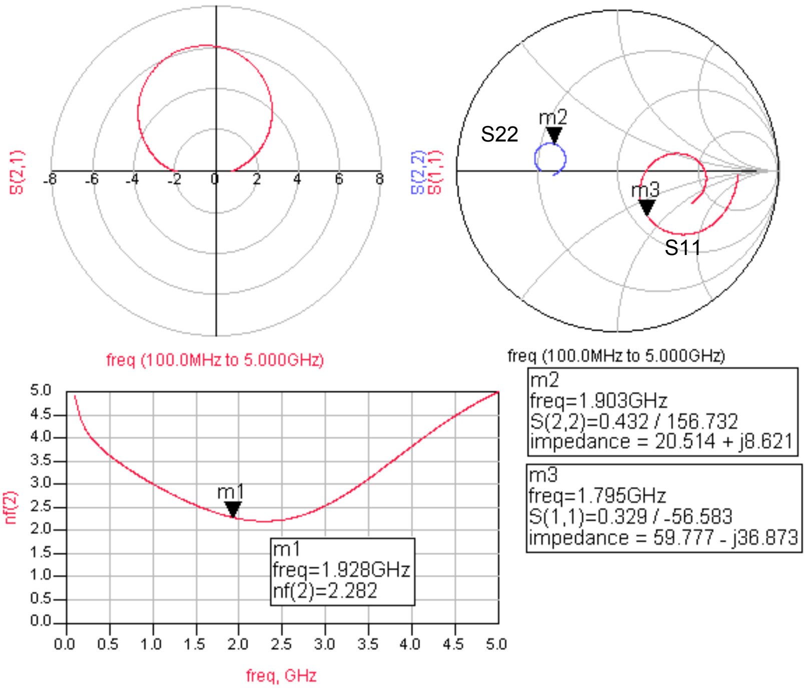


Figure 2.34 – Performance of Two FET Gain-Block with Cgs Tuning Inductors

2.4 Complete Amplifier Design

The circuit components chosen to build a lossless-feedback amplifier are the transmission line, discrete component coupler shown in Figure 2.16 and the two-FET gain-block as shown in Figure 2.31. This coupler is the smallest of the couplers investigated and has a reasonably low loss in the input transmission path, as well as an acceptable although greater loss in the output transmission path. The path with the lower loss path is selected as the input path in order to minimize the affect on the amplifier noise figure. The coupler requires a small amount of coupling between the windings to function correctly, but this is not considered impractical.

The starting circuit for the design of the amplifier is shown in Figure 2.31. The forward gain peaks at 18dB at 1.8GHz and the NF has a minimum of 3dB, this is high although acceptable and the amplifier is unconditionally stable. The phase rotation of the forward transmission path (S21) is not perfectly inverting and has approximately 30-degrees of unwanted phase rotation at 1.8GHz and this will need to compensated in the design of the coupler for best stability.

The method to compensate for the amplifier unwanted phase rotation is to design the RF-directional coupler to work above the required operating frequency. In doing so, this will result in a leading phase response from the coupler at the frequency of interest. Simulations have shown that a coupler designed at 2.5GHz will achieve the necessary phase rotation without a large variation in the coupled power at the frequency of interest, which may result in an unacceptable amplifier frequency response.

2.4.1 Frequency Choice

The operating frequency is an important design consideration. It is limited at the low frequency end by the performance of the RF directional coupler. Operating below 1.5GHz will make this circuit large and have high forward path loss. Operation at the high frequency end is limited by the gain that can be obtained from the transistor stages, where it is necessary to obtain a minimum of 17dB of gain with the minimum of transistors. The optimum frequency is between 1.5 to 2GHz.

2.4.2 Discrete Component Coupler at 2.5GHz

The required coupling power for the amplifier is 14dB at 2.5GHz; the circuit is shown in Figure 2.35 and the results in Figure 2.36.

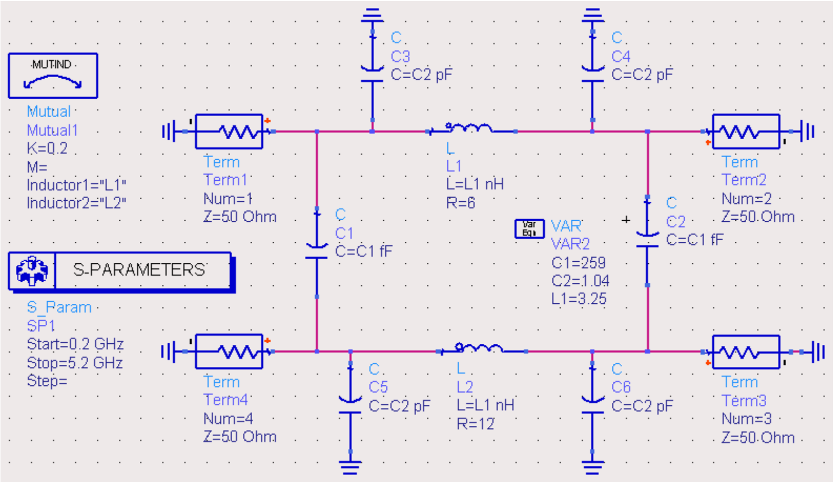

MUTIND
Mutual
Mutual1
K=0.2
M=
Inductor1="L1"
Inductor2="L2"
S-PARAMETERS
S_Param
SP1
Start=0.2 GHz
Stop=5.2 GHz
Step=
Term
Term1
Num=1
Z=50 Ohm
Term
Term4
Num=4
Z=50 Ohm
C
C3
C=C2 pF
C
C4
C=C2 pF
L
L1
L=L1 nH
R=6
C
C1
C=C1 fF
VAR
VAR2
C1=259
C2=1.04
L1=3.25
C
C2
C=C1 fF
Term
Term2
Num=2
Z=50 Ohm
C
C5
C=C2 pF
L
L2
L=L1 nH
R=12
C
C6
C=C2 pF
Term
Term3
Num=3
Z=50 Ohm

Figure 2.35 – 14dB 2.5GHz Discrete Component Coupler

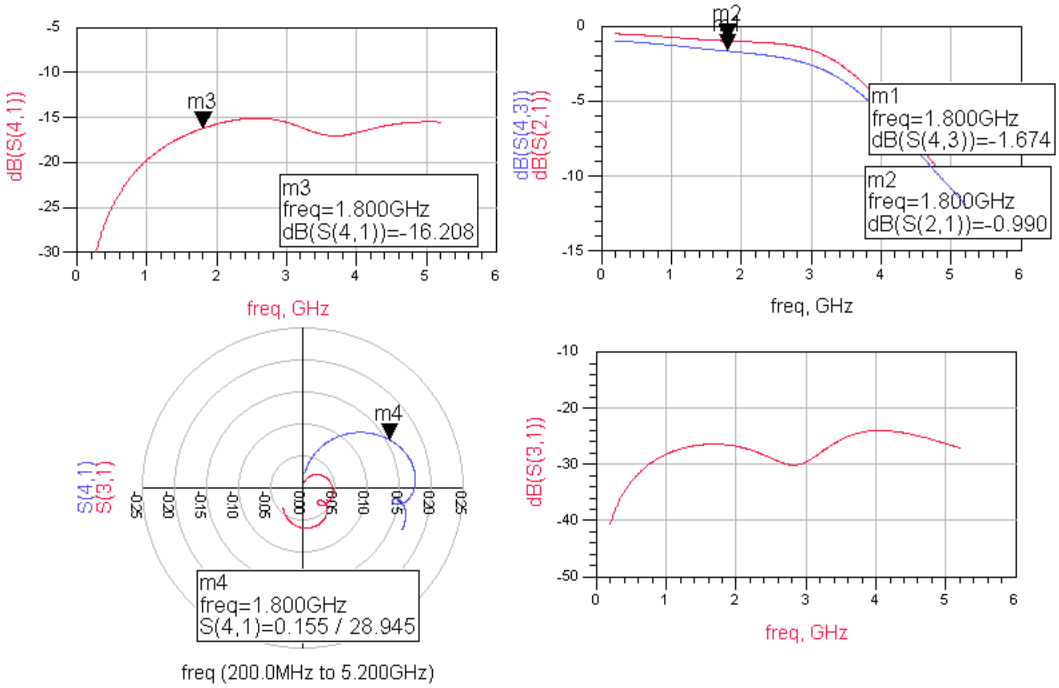


Figure 2.36 – Simulation Results for 14dB 2.5GHz Discrete Component Coupler

The coupling level is found by simulating the coupler as part of the amplifier and it depends on the overall gain required by the amplifier and the gain provided by the gain-block. The forward path transmission loss (S21) of this coupler is 1dB at 1.8GHz, and the amplifier output path loss (S43) is simulated to be 1.67dB. These losses are estimated by adding appropriate resistance in series with each transformer windings to simulate the expected inductor Q of the IC process. The forward transmission path is on the metal-5 layer of the IC, which is 2um thick and the return winding on the metal-4 layer and 0.6um thick. Further details of the IC construction can be found in section 3.1.

Simulations show the coupling level (S41), which is important for the amplifier stability and gain flatness to have a leading phase shift of about 29 degrees at 1.8GHz. The variation in coupling power has is approximately 1.5dB from 1.5 to 2GHz, although it is difficult to estimate how this will affect the gain of the complete amplifier.

2.4.3 Complete Lossless Feedback Amplifier

The gain-block and coupler are assembled together to build the complete amplifier in Figure 2.37 with the results presented in Figure 2.38. The Noise figure for the complete amplifier is simulated to be 3.5dB, which corresponds to adding the NF of the gain block at 2.5dB, plus an extra 1dB of loss in the forward path of the coupler. The Gain over the frequency range from 1.5GHz to 2GHz varies from 8.6dB to 7.5dB, this has more variation than is desired, but is not a bad starting point. The input and output impedance are very good considering the input and output impedance of the gain-block without the coupler shown in Figure 2.32.

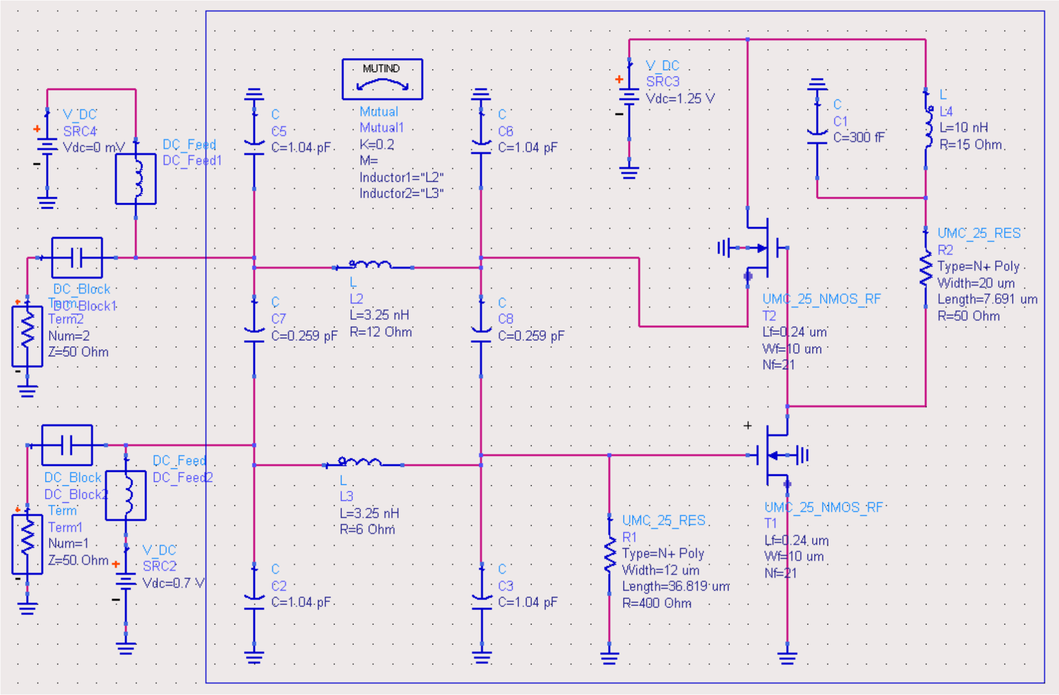

V_DC
SRC4
Vdc=0 mV
DC_Feed
DC_Feed1
DC_Block
DC_Block1
Term
Term2
Num=2
Z=50 Ohm
DC_Block
DC_Block2
Term
Term1
Num=1
Z=50 Ohm
DC_Feed
DC_Feed2
V_DC
SRC2
Vdc=0.7 V
C
C5
C=1.04 pF
MUTIND
Mutual
Mutual1
K=0.2
M=
Inductor1="L2"
Inductor2="L3"
C
C6
C=1.04 pF
L
L2
L=3.25 nH
R=12 Ohm
C
C7
C=0.259 pF
C
C8
C=0.259 pF
L
L3
L=3.25 nH
R=6 Ohm
C
C2
C=1.04 pF
C
C3
C=1.04 pF
V_DC
SRC3
Vdc=1.25 V
C
C1
C=300 fF
L
L4
L=10 nH
R=15 Ohm
UMC_25_RES
R2
Type=N+ Poly
Width=20 um
Length=7.691 um
R=50 Ohm
UMC_25_NMOS_RF
T2
Lf=0.24 um
Wf=10 um
Nf=21
UMC_25_RES
R1
Type=N+ Poly
Width=12 um
Length=36.819 um
R=400 Ohm
UMC_25_NMOS_RF
T1
Lf=0.24 um
Wf=10 um
Nf=21

Figure 2.37 – Lossless Feedback Amplifier

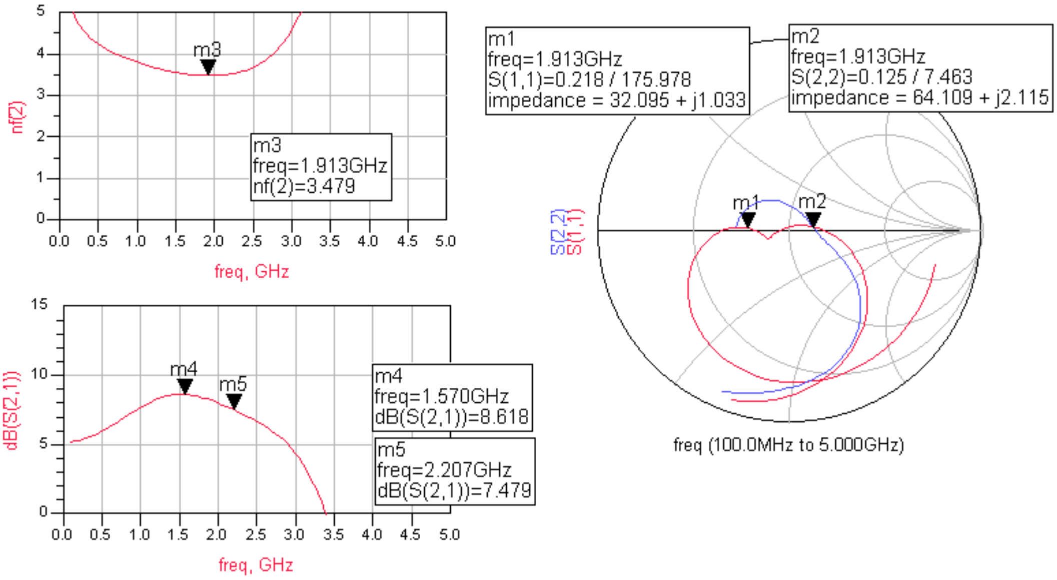


Figure 2.38 – Performance of Lossless Feedback Amplifier

Of particular concern is the stability of this amplifier and these simulations show the amplifier to be unconditionally stable from 0 to 5GHz. All the different metrics for stability are shown here in Figure 2.39 including μ and μ', as well as the conventional Rollet's calculation of stability and finally the input and output stability circles. All indicate unconditional stability.

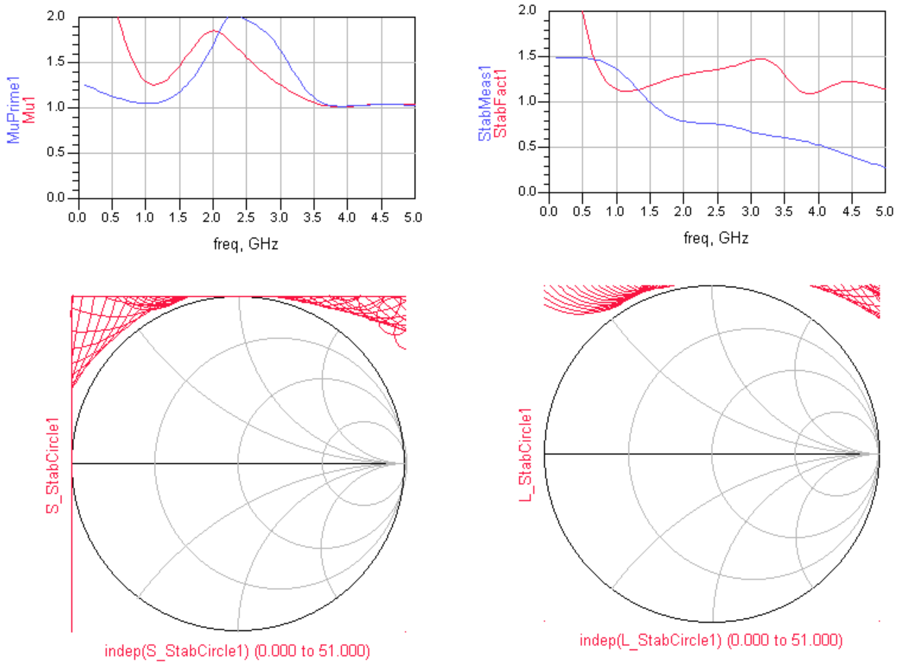


Figure 2.39 – Measures of Amplifier Stability

Adding the feedback around the amplifier is expected to improve the amplifier linearity and increase the IIP3. A simulation is set to measure the IIP3 across the band, both with and without the coupler. The improvement in IIP3 is shown in Figure 2.40 and shows a minimum of 10dB improvement can be expected from 1.2 to 2.4GHz.

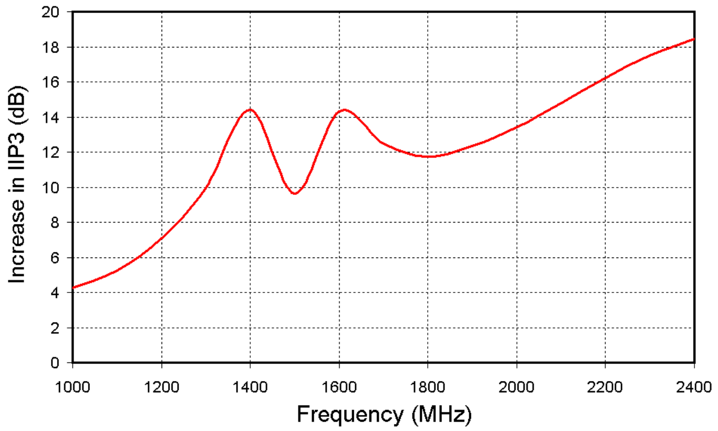


Figure 2.40 – Increase in IIP3 when Coupler is added

There are two other measures of linearity that need to be considered in the design; these are the 1dB compression point and the phase-power response, both of which are shown in Figure 2.41. The 1dB compression point of the amplifier is found to be worse by just over 0.2dB from 5.7dBm to 5.5dBm when the coupler is added. This actually indicates that the 1dB compression point out of the gain-block has improved by a small amount, as the output path loss in the coupler at 1.67dBm needs to be considered. If we are able to find a coupler without loss, then we would see a small improvement in this 1dB-compression point as predicted.

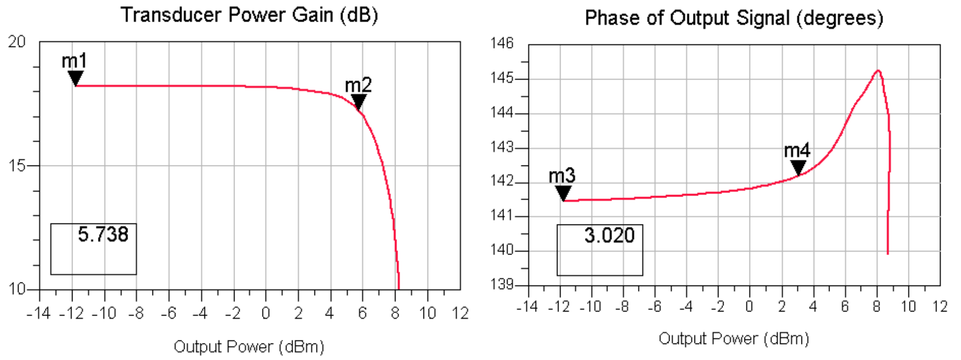


Figure 2.41a – Gain Compression & AM-PM Characteristics of Non-Feedback Amplifier

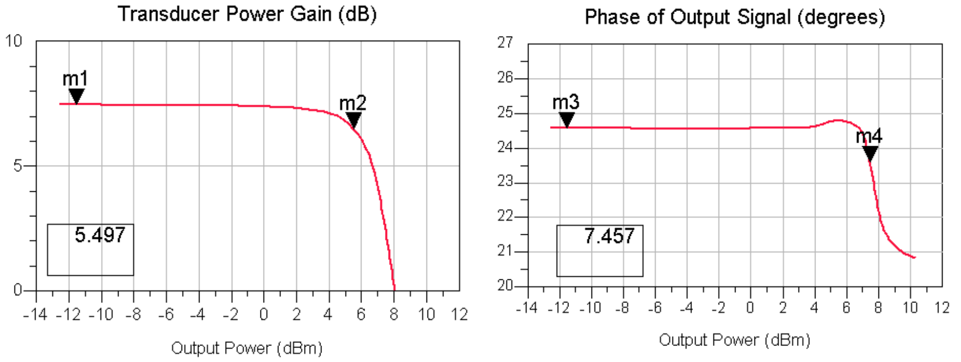


Figure 2.41b – Gain Compression & AM-PM Characteristics of Lossless Feedback Amplifier

The phase response of the amplifier has also improved with the 1° phase error point increasing from 3dBm to 7.5dBm, and this is now higher than the output 1dB compression point.

3 DESIGN OF THE INTEGRATED CIRCUIT

3.1 IC Construction

The starting point for the design of integrated circuit is to understand the IC construction. A figure that shows this for the process used in this project is given in a document by UMC [19] and duplicated here in Figure 3.1. The resistivity and dimensions are supplied in another document [16]. The top metal M5 is 2µm thick and has a resistance from 0.01 to 0.03-Ohm/sq; with 0.02-Ohm/sq used in the simulations. The other metal layers are 0.6µm thick and have a resistance from 0.035 to 0.075-Ohm/sq; with 0.053-Ohm/sq used in the simulations.

There is approximately 1um of SiO_2 between each of the metal layers, and between 7.4 and 8.1µm from the bottom of the M5-metal layer to the substrate, with the substrate slightly doped to have an average resistivity of 20-Ohm-cm. The substrate losses are important in the design of the inductors, as the induced losses into the substrate account for approximately half of the effective series resistance of a inductor, the other half being attributed to the resistive losses from the metal.

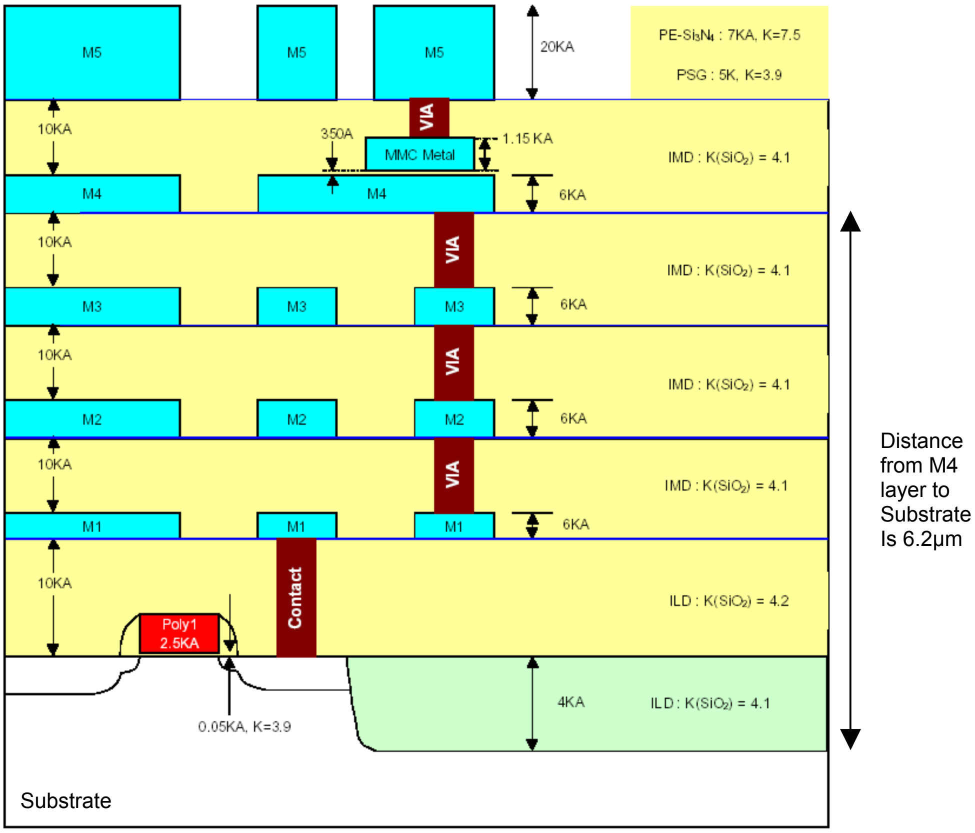

M5
M5
M5
20KA
PE-Si3N4 : 7KA, K=7.5
PSG : 5K, K=3.9
10KA
VIA
350A
MMC Metal
1.15 KA
IMD : K(SiO2) = 4.1
M4
M4
6KA
10KA
VIA
IMD : K(SiO2) = 4.1
M3
M3
M3
6KA
10KA
VIA
IMD : K(SiO2) = 4.1
M2
M2
M2
6KA
10KA
VIA
IMD : K(SiO2) = 4.1
M1
M1
M1
6KA
10KA
Contact
ILD : K(SiO2) = 4.2
Poly1
2.5KA
4KA
ILD : K(SiO2) = 4.1
0.05KA, K=3.9
Substrate
Distance
from M4
layer to
Substrate
Is 6.2µm

Figure 3.1 – UMC IC Construction [19].
The layers M are metal layers

An ambiguity was noticed between the UMC reference documents that define the spacing between the MMC metal layer and M4. Figure 3.1 shows this gap to be 350A (0.035µm) whereas the second reference document [16] specifies that this gap to be between 450A to 550A (0.045µm to 0.055µm). This discrepancy becomes important when the capacitor values are calculated in section 3.3.1, when the value of 500A (0.05µm) is used.

Section 3.2 describes the construction of three subassemblies, both RF directional couplers and the gain block. Section 3.3 describes the construction of the passive components.

3.2 Sub Assemblies

3.2.1 Discrete Component Coupler

The discrete component coupler is designed in a number of sages; firstly the inductance of the top layer is calculated and simulated using the Momentum simulator [13]. An inductance value of 3.2nH is required for the design and as a starting point the inner diameter of a square inductor is estimated using the MathCAD sheet on page 91, which suggests an inner diameter of 125µm, an outer diameter of 233µm and with 3.25 turns of 13µm line-width and 2µm spacing. The starting estimate can be verified using a web page from the Stanford University site, which can be found at http://smirc.stanford.edu/spiralcalc.html.

This inductor is then optimized using Momentum to get the dimensions shown in Figure 3.2. The momentum calculations are made without a guard ring that would normally circle the inductor in IC construction, with the second port shown on the right in this diagram as the ground return. In addition, even though this inductor is on metal-5 which is 2µm thick, this thickness is not constructed as part of the simulation with the metal layers simulated as thin tracks.

The inductor shape was based on the ADS circuit component 'MRINDNBR' shown in Figure 3.3. The final dimensions were Ns=13, L1=270µm, L2=230µm, L3=170µm, W=13µm and S=2µm, and this inductor simulates to be 3nH with a series resistance of 4.9-Ohms, or a corresponding Q of 7.75 at 2GHz.

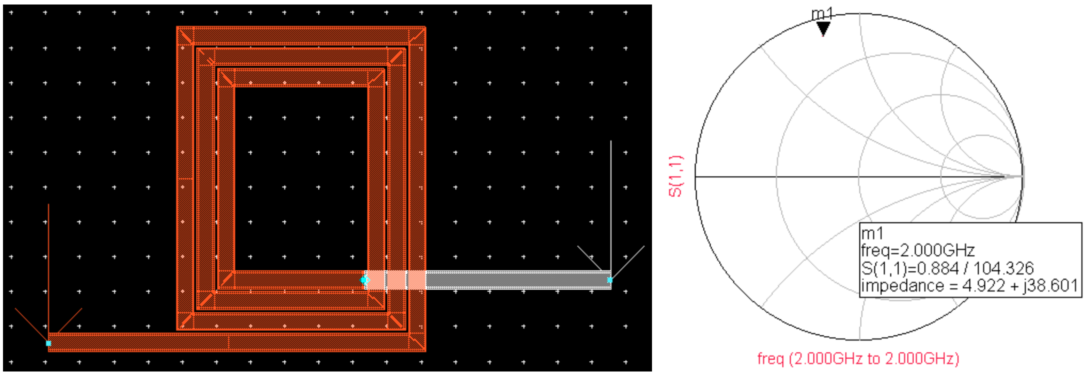


Figure 3.2 – Momentum Design of Inductor
In this simulation the right-hand port is earthed

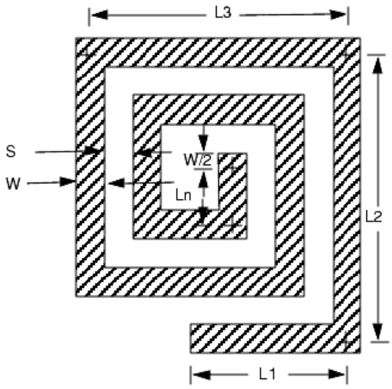


Figure 3.3 – (MRINDNBR) Inductor Definitions

It is possible to achieve an inductor with a higher Q if a multi-sided design had been chosen for the design, for example a spiral, octagon or a hexagon. The rectangle inductor was chosen in preference for a number of reasons. Firstly the simulation time is less, the inductor in Figure 3.2

takes just a few minutes to simulate compared to 30 minutes for a spiral. Furthermore when two spiral inductors are laid on top of each other to form a transformer, the simulation can take at least 24-hours. The second reason is the ease of construction using Cadence; this tool prefers orthogonal tracking, with 45-degree tracking acceptable but time-consuming and with spiral tracking less acceptable creating a large number of DRC errors.

The next step is to overlay the two inductors, one on metal layer-5 and the other on metal layer 4, and to simulate the transformer using Momentum with a guard ring around the full design. In this example Momentum is set to simulate up to 10GHz with 400-cells per wavelength. The resulting 4-port S-parameters are exported and further simulated with the addition of appropriate capacitor values in a second simulation circuit. These results were compared to the 'ideal' model found in Figure 2.35, and the overlap of the two inductors are iteratively adjusted to achieve the same response. This process takes several days as each Momentum simulation takes 12-hours to run. The final layout of the coupler windings is shown in Figure 3.4.

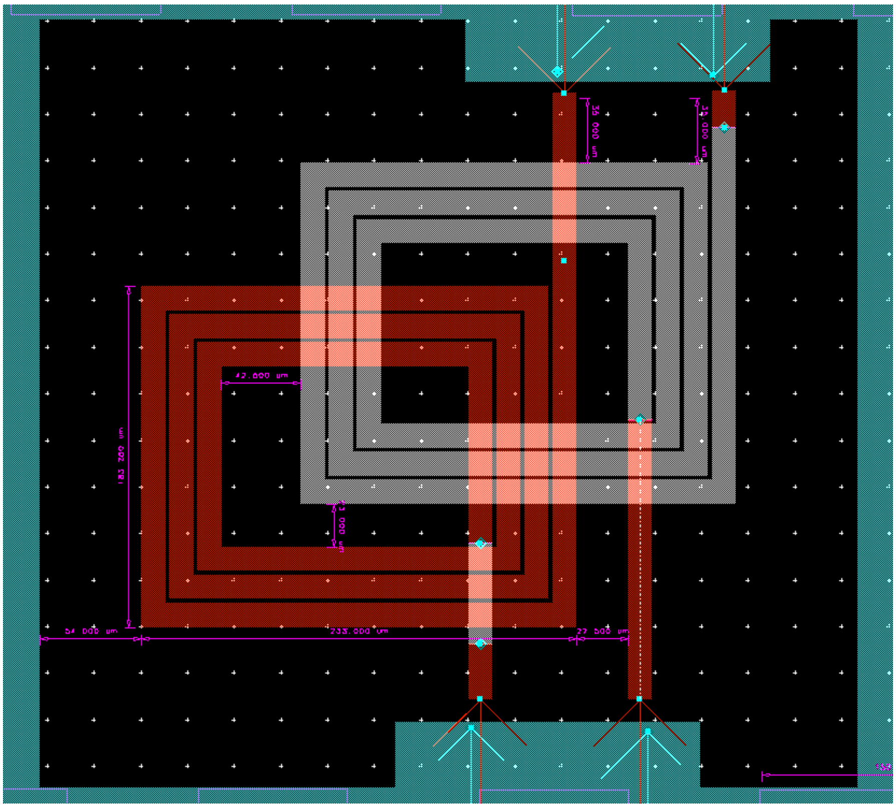


**Figure 3.4 – Momentum Simulation of Discrete Component Coupler.
This Figure shows the two Inductors that form the coupler.
There are four RF ports, with a ground connection associated with each.**

A few dimensions are shown in this figure. Each winding has an outside dimension of 233µm by 183µm. The two windings are offset by 23µm & 42.5µm to each other and the earth plane on M1 is 55µm at the closest point to the windings.

It is worth at this stage showing the substrate construction used in the Momentum simulation. This is shown in Figure 3.5 and should be compared to the IC construction shown in Figure 3.1. The metal layers are approximated to thin lines and the distance from the M4 layer to the substrate is given by UMC [16] to be 6.2µm.

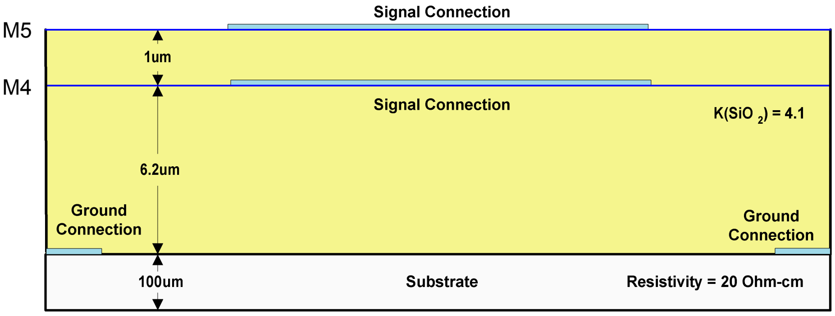

Signal Connection
M5
1um
M4
Signal Connection
K(SiO $_2$) = 4.1
6.2um
Ground Connection
Ground Connection
100um
Substrate
Resistivity = 20 Ohm-cm

Figure 3.5 – Momentum Substrate Construction for Design of Couplers

The Momentum simulation generates a 4-port S-parameter file and this is imported into the second ADS simulation sheet shown in Figure 3.6 where the capacitors are added and results for this are shown in Figure 3.7. It is worth taking a few moments to compare this simulation with the one in Figure 2.36 on page 32, made using ideal components. Both results look similar; perhaps the most important parameter to compare is the S41 phase angle, which is 27.4° in this simulation compared to 29° for the ideal components.

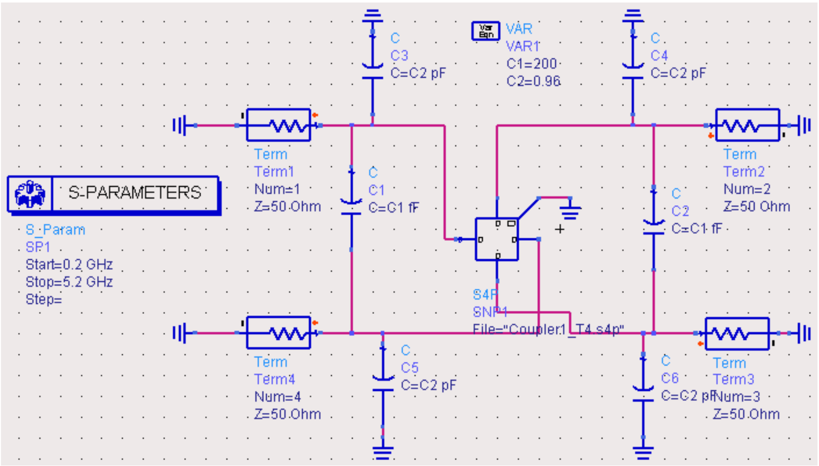

C
C3
C=C2 pF
VAR
VAR1
C1=200
C2=0.96
C
C4
C=C2 pF
S-PARAMETERS
S_Param
SP1
Start=0.2 GHz
Stop=5.2 GHz
Step=
Term
Term1
Num=1
Z=50 Ohm
C
C1
C=C1 fF
C
C2
C=C1 fF
Term
Term2
Num=2
Z=50 Ohm
S4P
SNP1
File="Coupler1_T4.s4p"
Term
Term4
Num=4
Z=50 Ohm
C
C5
C=C2 pF
C
C6
C=C2 pF
Term
Term3
Num=3
Z=50 Ohm

Figure 3.6– 14dB 2.5GHz Discrete Component Coupler

As part of the design the inductors have a capacitance to the ground plane and a capacitance to each other that needs to be compensated for in the design. The inter-winding capacitance is estimated using the simple capacitance equation to be 270fF and this is divided by two and subtracted from each of the two discrete capacitors to give 200fF as the final design value. In the same way the capacitance to ground is estimated, divided by two and subtracted from the capacitance to ground. The final capacitor values used in the simulation and in the construction of the IC are 200fF and 960fF.

The circuit can now be laid out using Cadence [24], with the final layout shown in Figure 3.8. Two-off 5-pin differential probes are used for the signal paths with short tracks to the 0.96pF capacitors that go to ground. The standard UMC capacitor construction was not used in this layout as these have a large keep-out region and would have been difficult to place close enough together to make the circuit work. Furthermore the 0.96pF capacitors are required to connect directly to the ground plane on the M1 metal layer and the standard capacitors do not do this. A full description of the capacitor construction can be found in section 3.3.1.

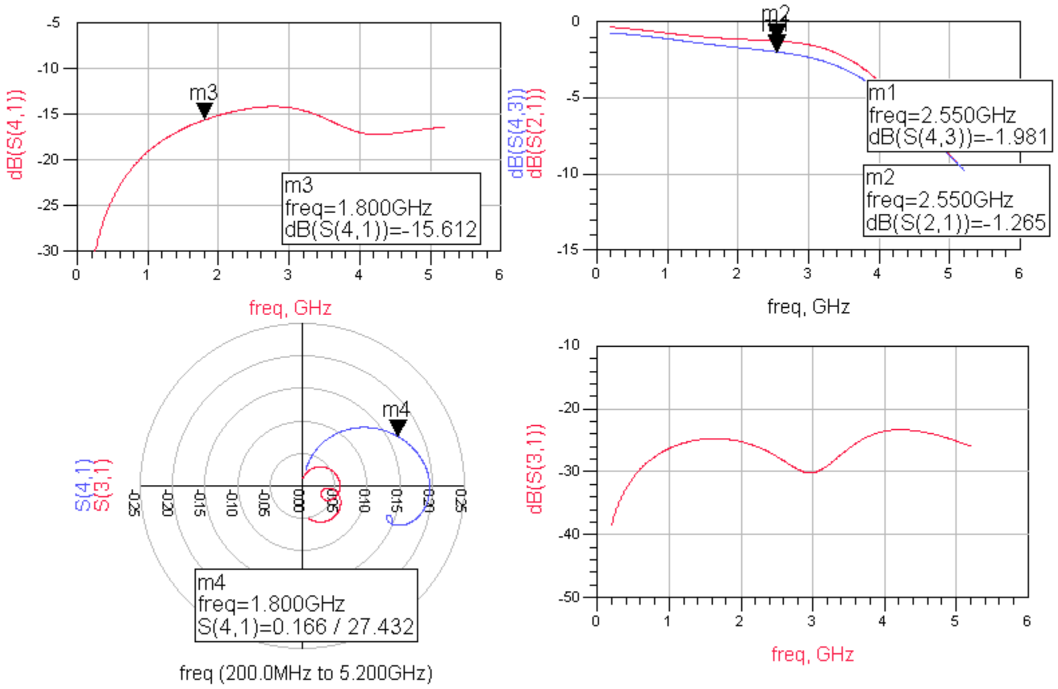


Figure 3.7– Simulation Results for 14dB 2.5GHz Discrete Component Coupler

The layout is kept as close to the Momentum simulation as possible. Both inductors are drawn as a series of rectangles, with their XY coordinates mathematically calculated and entered into the rectangle's property boxes. The M1-layer (light-blue) is used for the earth plane and is built-up as a series of strip to try to meet a design rule that limits the maximum dimension of any metal layer. Even with this slicing the DRC fails, but the layout is considered acceptable for fabrication. The coupler occupies an area of 450μm by 400μm not including probe pads. The layer definitions can be found in reference [24].

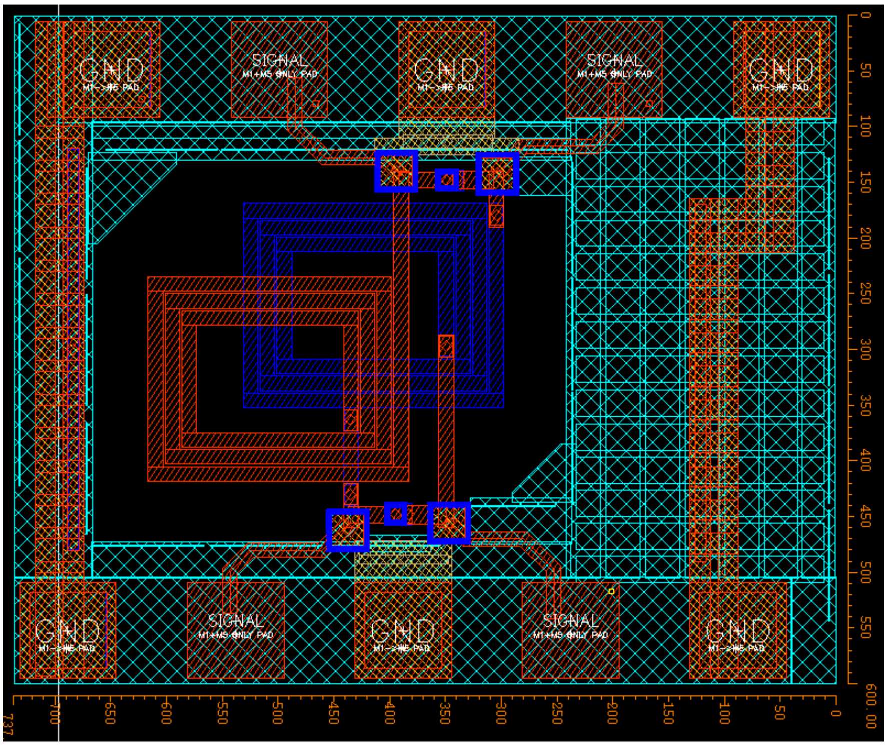

GND
M1+M6 PAD
SIGNAL
M1+M6 ONLY PAD
GND
M1+M6 PAD
SIGNAL
M1+M6 ONLY PAD
GND
M1+M6 PAD
GND
M1+M6 PAD
SIGNAL
M1+M6 ONLY PAD
GND
M1+M6 PAD
SIGNAL
M1+M6 ONLY PAD
GND
M1+M6 PAD
0 50 100 150 200 250 300 350 400 450 500 550 600.00
737 700 650 600 550 500 450 400 350 300 250 200 150 100 50 0

Figure 3.8 – Layout of the 14dB 2.5GHz Discrete Component Coupler

3.2.2 Transformer Coupler

Although not required as part of the proposed lossless-feedback amplifier, the transformer coupler described in section 2.2.3 is to be designed and fabricated. This coupler looks to be a promising solution for a wideband coupler and to the authors knowledge such a design has not been built on an IC before. The design steps are similar to the transmission-line coupler, starting by simulating and optimizing the inductance of the primary winding, and then adding the secondary winding.

The coupler is made up of two independent transformers and the winding ratio of these does not need to be equal for the coupler to work, although it helps in the construction and layout symmetry if they are. The design equations are described in a paper by Kajfez [14] and analyzed on a MathCAD sheet on page 93. In this construction the turn's ratio for both transformers is set to 3.5, which should result in an 11dB coupler.

The Momentum layout is shown in Figure 3.9, the primary winding consists of two turns of 27µm width and 10.5µm spacing, with 257µm as the length of the outer winding. The secondary winding is on metal-4 and this has a track width of 8µm and a spacing of 3µm with 260µm as the length of the outer winding to the turning point. This results in a maximum outside dimension of 268µm for the transformer assembly. The secondary winding has 7-turns.

The momentum substrate construction for this coupler is identical to the construction used for the discrete component coupler shown in Figure 3.5.

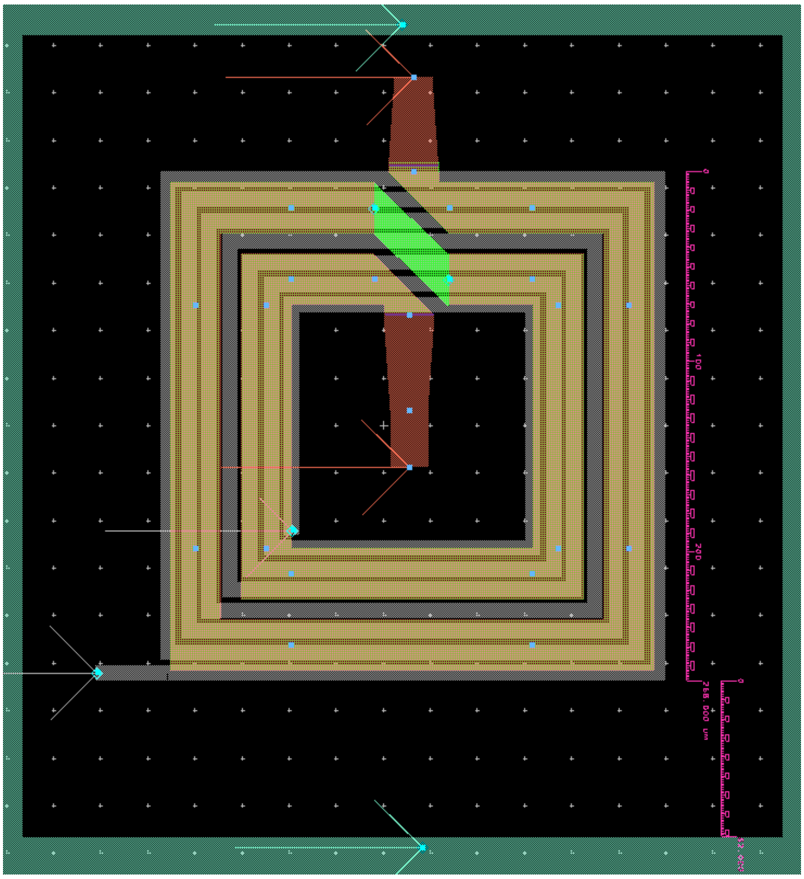


Figure 3.9 – Detail of Transformer Coupler Winding

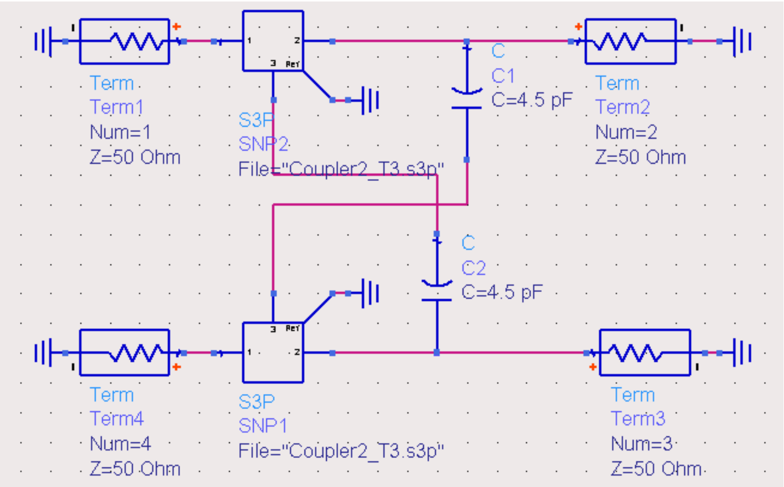

Term
Term1
Num=1
Z=50 Ohm
S3P
SNP2
File="Coupler2_T3.s3p"
C
C1
C=4.5 pF
Term
Term2
Num=2
Z=50 Ohm
C
C2
C=4.5 pF
Term
Term4
Num=4
Z=50 Ohm
S3P
SNP1
File="Coupler2_T3.s3p"
Term
Term3
Num=3
Z=50 Ohm

Figure 3.10 – Transformer Coupler

As with the previous coupler design, the results from Momentum simulator are exported as an S-parameter file and then simulated with the capacitors added in a second simulation circuit shown in Figure 3.10, with the results shown in Figure 3.11. These results show a very broadband coupler is achievable. The coupling level is 12dB from 2GHz to 9GHz and the coupler has a good phase response especially at the lower frequencies when the phase response leads the 0º point. The losses in the forward and reverse paths are higher than expected at 1.48dB.

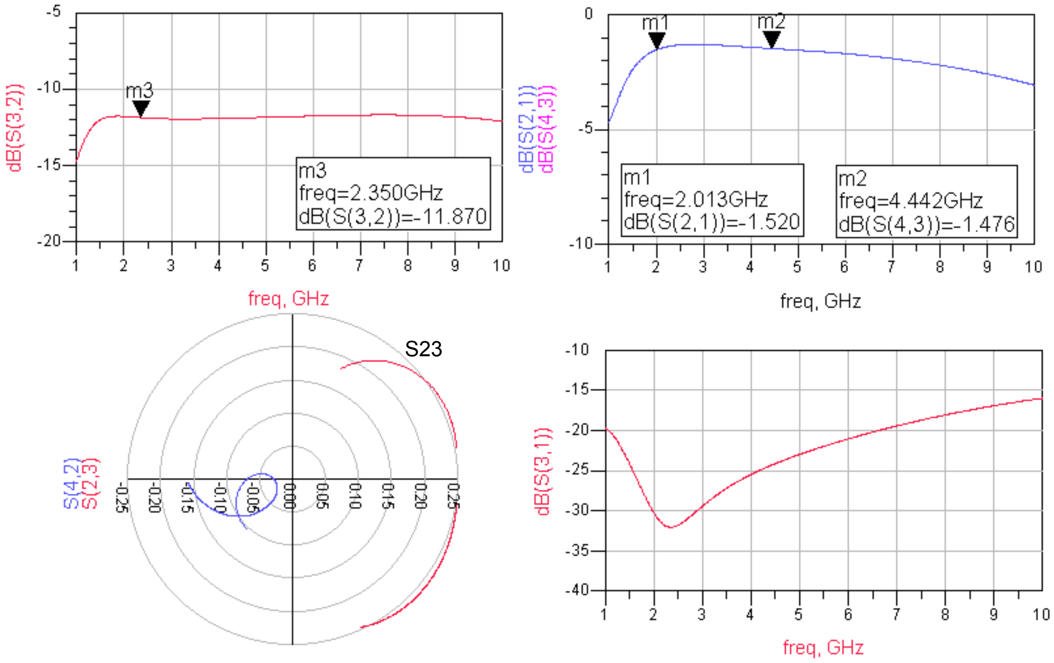


Figure 3.11 - Simulation Results for Transformer Coupler

Many simulations were made before getting to these results. The biggest challenge in the design is to achieve the close coupling between the primary and secondary winding that is essential for good operation. In order to optimize and understand the circuit performance a second simulation circuit is created using ‘ideal’ components and the results compared. The ‘ideal’ circuit is shown in Figure 3.12 with the results from this shown in Figure 3.13 and these compare well to the results from the Momentum simulation shown in Figure 3.11.

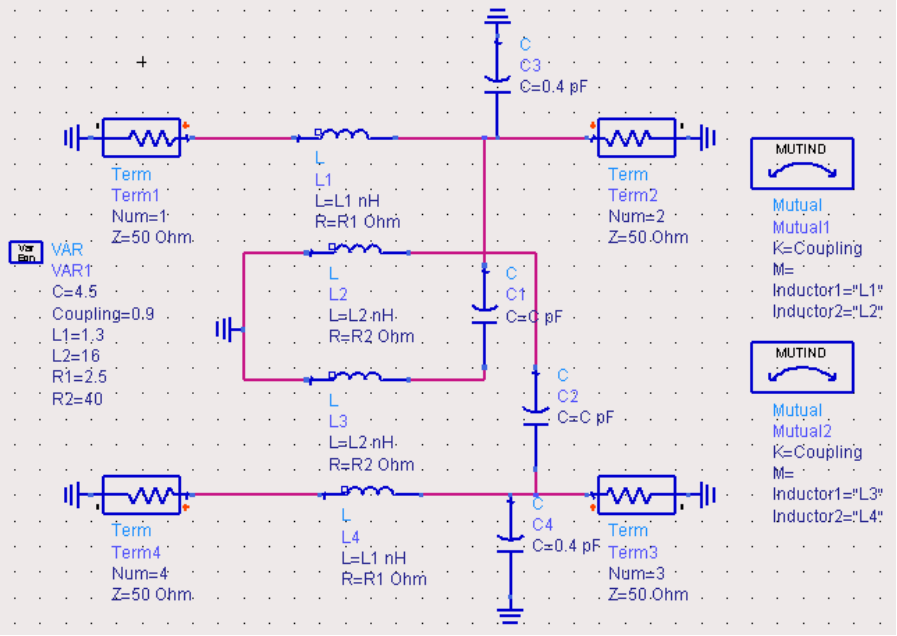

C
C3
C=0.4 pF
Term
Term1
Num=1
Z=50 Ohm
L
L1
L=L1 nH
R=R1 Ohm
Term
Term2
Num=2
Z=50 Ohm
MUTIND
Mutual
Mutual1
K=Coupling
M=
Inductor1="L1"
Inductor2="L2"
VAR
VAR1
C=4.5
Coupling=0.9
L1=1.3
L2=16
R1=2.5
R2=40
L
L2
L=L2 nH
R=R2 Ohm
C
C1
C=C pF
MUTIND
Mutual
Mutual2
K=Coupling
M=
Inductor1="L3"
Inductor2="L4"
C
C2
C=C pF
L
L3
L=L2 nH
R=R2 Ohm
Term
Term4
Num=4
Z=50 Ohm
L
L4
L=L1 nH
R=R1 Ohm
C
C4
C=0.4 pF
Term
Term3
Num=3
Z=50 Ohm

Figure 3.12 – Transformer Coupler with Ideal Components

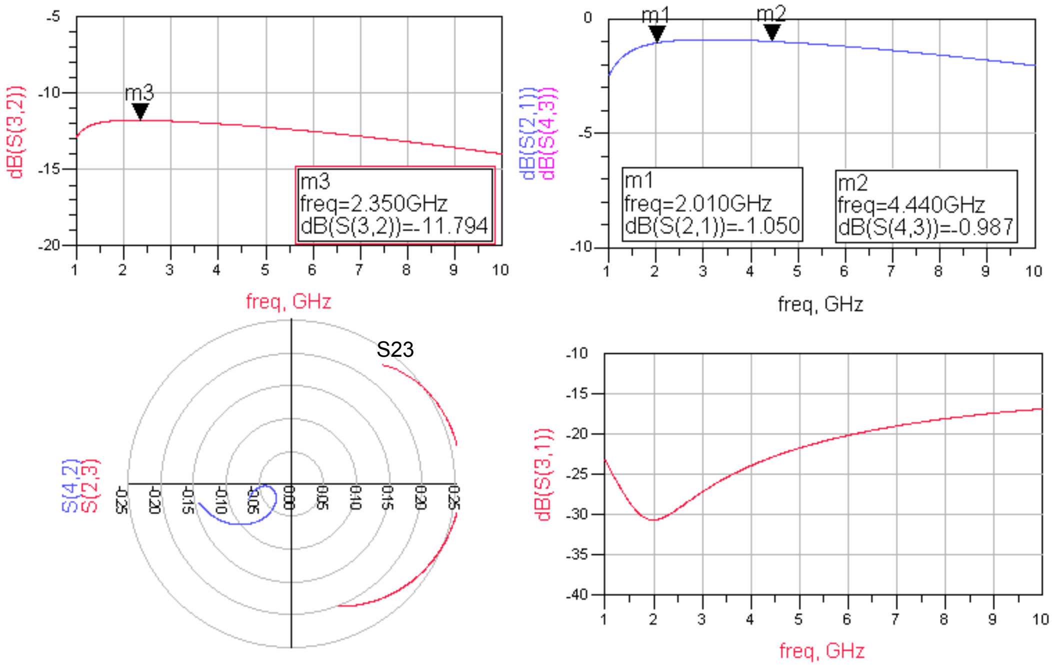


Figure 3.13 - Simulation Results for Transformer Coupler with Ideal Components

This ideal simulation implies that the transformer layout has achieved a high coupling of 0.9 between the windings, this is high but within a range that is considered achievable [28]. The ideal component coupler shows a loss of 1.128dB in the forward and reverse transmission paths whereas the Momentum simulation results show a loss of 1.48dB, the extra loss is attributed to the induced substrate losses and this has been shown in simulations with a lossless substrate.

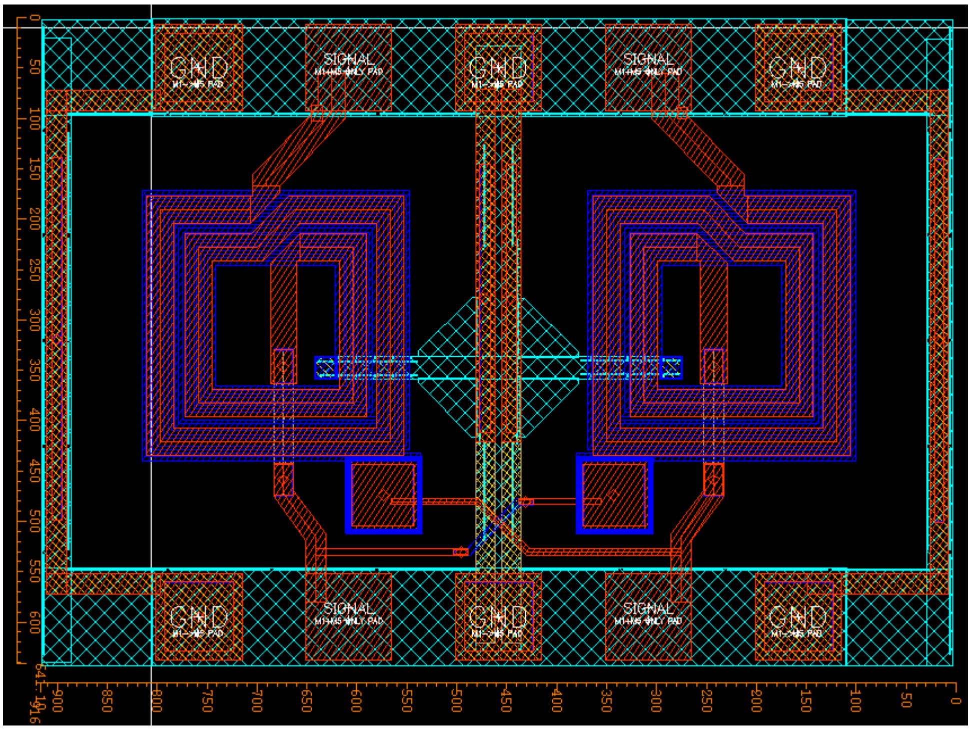

GND
SIGNAL
GND
SIGNAL
GND
GND
SIGNAL
GND
SIGNAL
GND
0
50
100
150
200
250
300
350
400
450
500
550
600
900
850
800
750
700
650
600
550
500
450
400
350
300
250
200
150
100
50
0

Figure 3.14 – Layout of the 12dB Transformer Coupler

The coupler circuit layout is shown in Figure 3.14 and uses two 5-pin RF probes to gain access to the circuit. The capacitors were created by copying and modifying the standard UMC 70µm (4.5pF) capacitor and is explained in more detail in Section 3.3.1. The two-turn inductor on the M5 layer is 27µm-wide and reduces to 20µm to track away to the RF pad. The transition between these two widths should be tapered but this was found to generate DRC errors in the layout and was changed to the abrupt change as seen here. The layer definitions can be found in reference [24].

3.2.3 Gain-Block

A separate layout is made of the Gain-Block to allow this part of the amplifier to be individually tested. The circuit is shown in Figure 3.15 and the components inside the rectangle are laid down on the IC as shown in Figure 3.18.

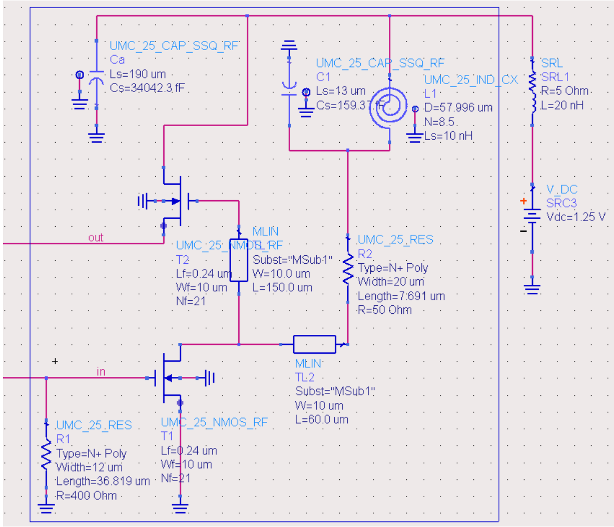

UMC_25_CAP_SSQ_RF
Ca
Ls=190 um
Cs=34042.3 fF
UMC_25_CAP_SSQ_RF
C1
Ls=13 um
Cs=159.37 fF
UMC_25_IND_CX
L1
D=57.996 um
N=8.5
Ls=10 nH
SRL
SRL1
R=5 Ohm
L=20 nH
V_DC
SRC3
Vdc=1.25 V
out
MLIN
UMC_25_NMOS_RF
T2
Lf=0.24 um
Wf=10 um
Nf=21
Subst="MSub1"
W=10.0 um
L=150.0 um
UMC_25_RES
R2
Type=N+ Poly
Width=20 um
Length=7.691 um
R=50 Ohm
in
MLIN
TL2
Subst="MSub1"
W=10 um
L=60.0 um
UMC_25_RES
R1
Type=N+ Poly
Width=12 um
Length=36.819 um
R=400 Ohm
UMC_25_NMOS_RF
T1
Lf=0.24 um
Wf=10 um
Nf=21

Figure 3.15 – Schematic of Gain-Block

The circuit is laid-out using two 5-pin probes, the one on the left of the circuit is to connect both the input and output RF signals, and the one on the right is to connect and monitor the dc power.

The spiral inductor from the UMC library dominates the layout. This inductor connects between the positive power-rail at the top of the layout, to the two FETs and has a 159fF capacitor at the bottom end to create the parallel tuned circuit. The standard UMC capacitor is used in the simulation, but the layout is built using a custom-built version of this capacitor that does not have the metal-1 clearance and has a better connection from the lower plate of the capacitor to the earth-plane on metal-1 layer.

The circuit resonance is created by the inductor (L1) and capacitor (C1), the frequency of this is critical to the operation of the amplifier and needs to be close to 1.8GHz. It is expected that a considerable reduction in circuit size could be made if the inductor is reduced in size, and some consideration was given to replacing the UMC inductor with a custom designed part that would be smaller and perhaps employing more than one metal layer. This approach was not adopted as the stray capacitance of the inductance would hard to quantify and would jeopardize the circuit operation. This option should be considered if the design is to be taken further.

The results of the simulation are shown in Figure 3.16. The tracking on the IC is simulated using Microstrip lines of appropriate width and length. A 20nH inductor is placed in series with the 1.25V supply to simulate the affect of an inductive connection to the power supply. It was found that if no decoupling capacitance is included on the IC, then the stability of the amplifier is badly compromised, as can be seen by the plots of µ and µ' in Figure 3.17.

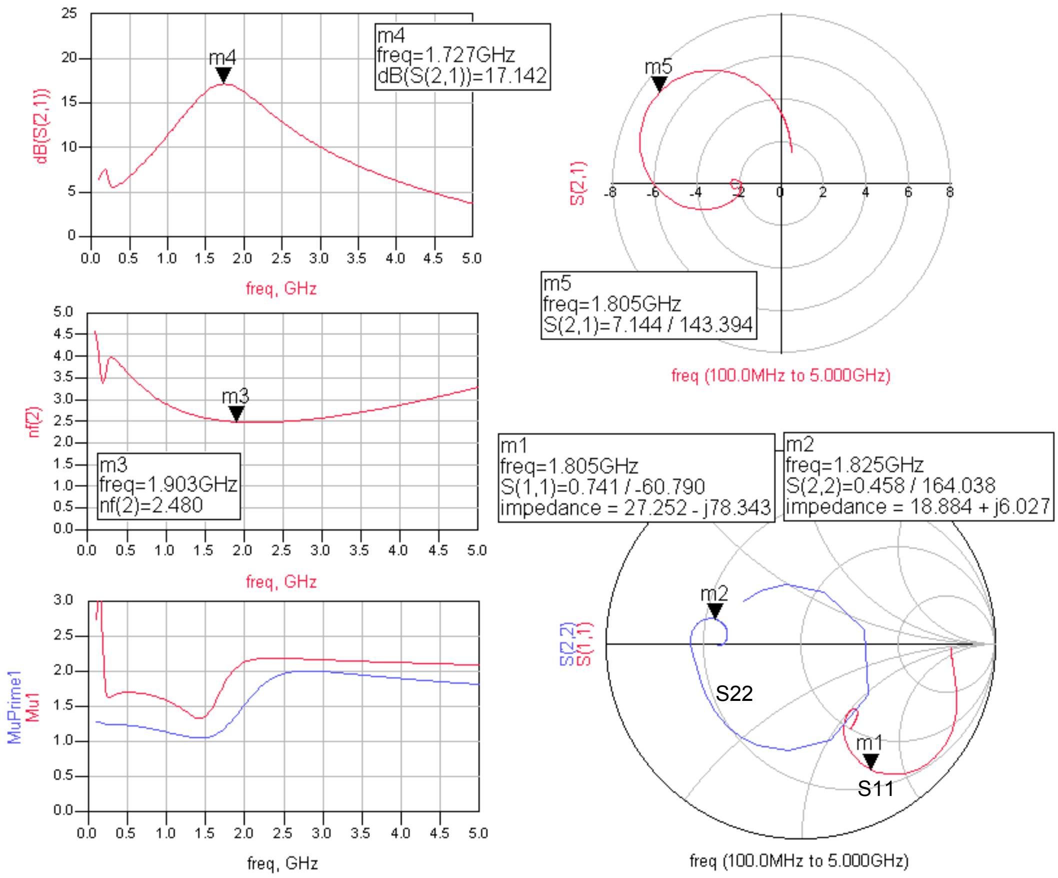


Figure 3.16 - Performance of Two-FET Gain-Block

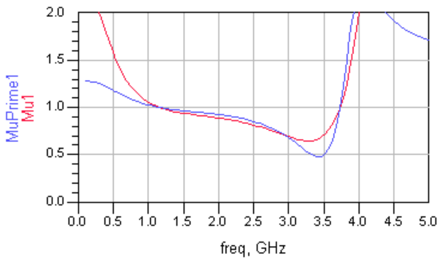


Figure 3.17 – Stability of the Two-FET Gain-Block without The on-chip Decoupling Capacitance

The solution to the stability problem is to include a large decoupling capacitor shown in top region above the spiral inductor in Figure 3.18. The decoupling is laid out as four similar sized capacitors of dimensions 100µm by 90µm, the capacitor is broken up in this way to comply with the maximum allowed dimensions of the MMC layer of 100µm by 100µm specified by the UMC process. The total capacitance is estimated to be 36pF, which is estimated from an equation from section 6 of the UMC reference [16] and duplicated below. There is expected to be a small inaccuracy with this calculation as the fringing capacitance is not included, but this is not important in the design.

$$Cap = 1\frac{fF}{\mu m^2} \cdot 4 \cdot (100\,\mu m \cdot 90\,\mu m) \equiv 36\,pF$$

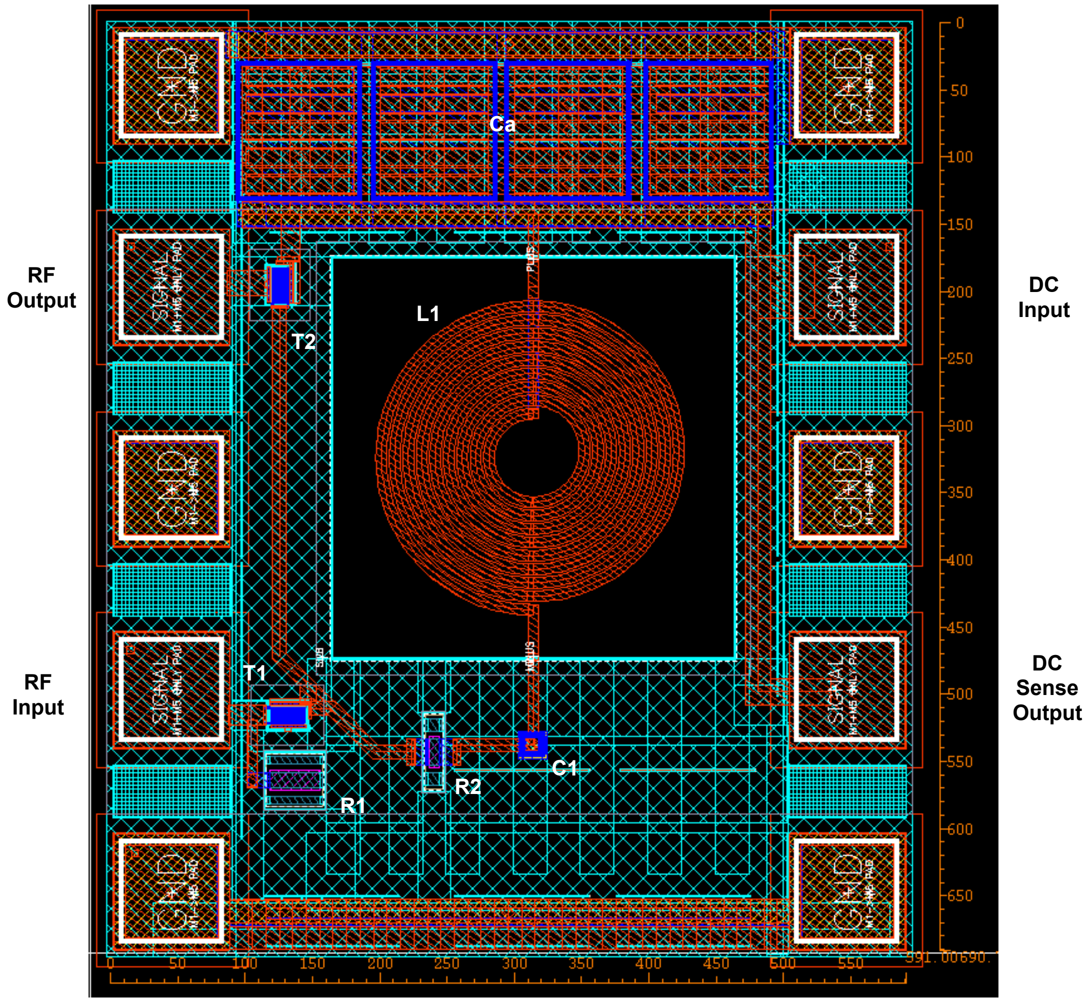

Ca
L1
T2
T1
R1
R2
C1
RF Output
RF Input
DC Input
DC Sense Output
GND
SIGNAL
0
50
100
150
200
250
300
350
400
450
500
550
600
650

Figure 3.18 - Layout of Two-FET Gain-Block

DC power is connected to the gain-block by using the 5-pin differential probe connector on the right hand side of the IC, with the top pad as the input power connection, and the bottom pad to sense the voltage back to the PSU. This approach is taken as the gain-block has no bias circuitry included and it is important for the voltages and currents to be accurately & repeatedly set for characterization of the amplifier.

The standard method for connecting power to an IC is to using a dc power probe. There are two problems with this that are overcome by using an RF probe in this unconventional manner. Firstly the contact resistance of the dc power probe is of a few ohms and is variable; and secondly it is not possible to put external decoupling capacitors close to the fixed end of the dc probe. Both of these problems could give problems during testing, possibly making the amplifier unstable.

To make use the sense connection close to the IC and to route this signal back to the PSU, a PCB was built to connect as close as possible to the SMA connectors on the 5-pin RF probe, and to place decoupling capacitors as close to these connectors as possible. The PCB for this is shown in Appendix B on page 98, and screen shots of the LabVIEW scripts as well as the PCB schematics can be found on the following pages.

3.3 Passive Components

3.3.1 Capacitors

Simulations of the circuit performance used the standard UMC capacitors, but these were not used in the layouts. There are two reasons for this, firstly the standard capacitor is large because of a clearance area that is required as shown in Figure 3.19. This clearance is required to minimize the stray capacitance from the bottom metal plate of the capacitor to the ground plane on the metal-1 layer, but causes the capacitor to be much larger than is desired. The capacitors in these circuits do not require a low stray from the capacitor bottom plate and this clearance area is not required.

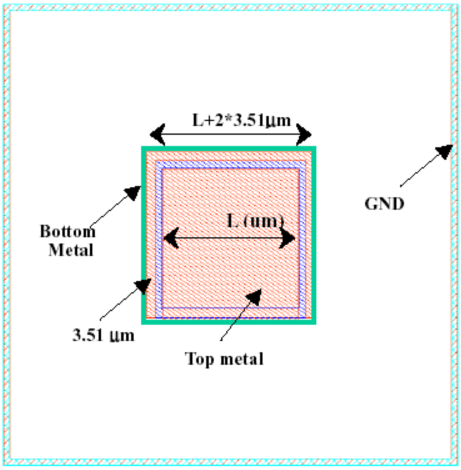


Figure 3.19 – Top View of UMC Capacitor Construction [15]

Secondly, both of the connections in the standard capacitor go to the top layer (M5) as shown in Figure 3.20. At least two of the capacitor required in the circuits do not require this and require one of the connections to go directly to the ground plane on the metal-1 layer. Redesigning the capacitor to allow a direct connection to metal-1 should help the final circuit be closer to the simulation model, as it will have less unwanted series inductance and lower resistance.

The new capacitor layout where one end is connected to the metal-1 ground plane is shown in Figure 3.21. A block of vias connects the metal area from M1 to M2 and M2 to M3, whereas the vias from M3 to M4 layers are only placed at the edge of the M4 layer, as otherwise it is feared that these will cause a ripple effect under the M4 layer and this may affect the capacitance value. Both capacitors have a large number of vias that connect from the M4 to the MMC layer. The guard ring is also included and is copied from the standard model.

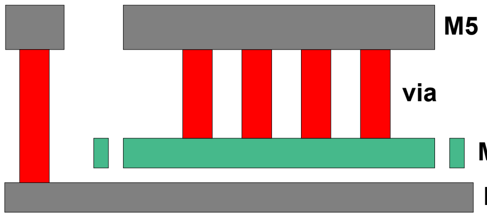


Figure 3.20 – Side View Diagram of UMC Capacitor Construction [15]

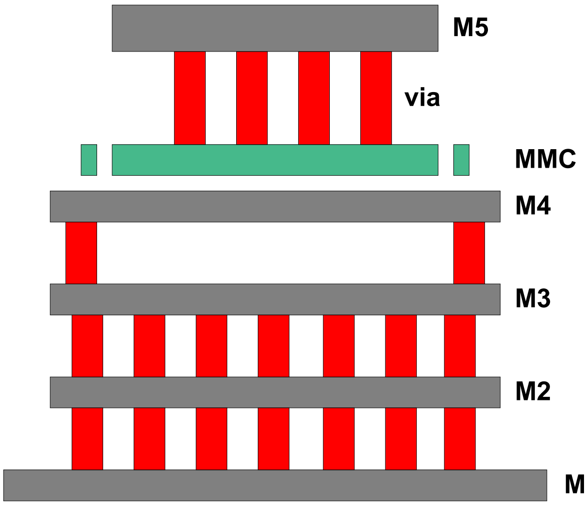


Figure 3.21 – Side View Diagram of actual Capacitor Construction Showing Ground Connection on M1

The designs of the capacitors used in the circuits are shown in Figure 3.22. The dimensions for each capacitor are calculated according to the formula given UMC [15] Table 4-3 and shown below.

$$Cs = 0.943 \cdot \frac{fF}{\mu m^2} \cdot Ls^2$$

An ambiguity was noticed between two UMC reference documents, regarding the spacing between the MMC layer and M4. The Figure 3.1 taken from reference [19] shows this gap to be 350A (0.035µm) whereas a second reference document [16] specifies this gap to be between 450A to 550A (0.045µm to 0.055µm). A value of 0.05µm is used for the calculations in the MathCAD sheet on page 89 that calculates the capacitance according to a number of standard formulas and with the UMC formula included for comparison. The UMC calculation gives a value substantially higher than the values obtained from other standard capacitance equations.

An interesting observation can be made by calculating the capacitor plate separation from the equation above using the simple capacitance model with a permittivity of SiO_2 at 4.1 and ignoring fringing affects. This calculates the spacing between the MMC and M4 layers to be 0.0385µm, which is between the dimensions presented in the reference documents.

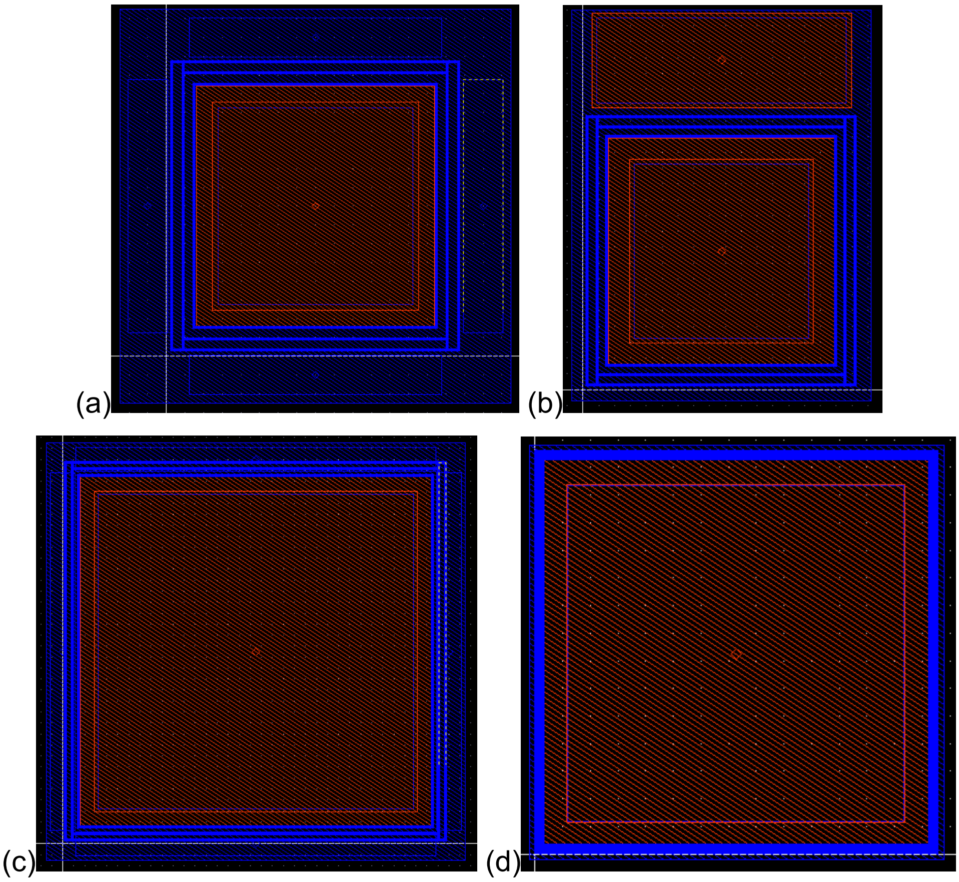


**Figure 3.22 – Capacitor Designs used in the Circuits:
(a) 13µm, (b) 14.5µm, (c) 32µm, (d) 70µm**

To clarify the situation several Momentum simulations were carried out on a 32µm side-length capacitor over a variety of cells/wavelength mesh densities. The structure of the capacitor is shown in Figures 3.23 and 3.24 and is identical to the standard UMC capacitor construction including the guard ring.

The simulation results are shown in Figure 3.25. The Momentum default setting of 30-cells/wavelength gives a capacitance value of 1.8pF with a Q of 4, which is very different from the UMC model [ref 15, table 4-3] of 0.965pF and a Q of 300. When the simulation resolution is increased, the capacitance value drops and become closer to the UMC value and the Q increases, but the results do not converge to the UMC values.

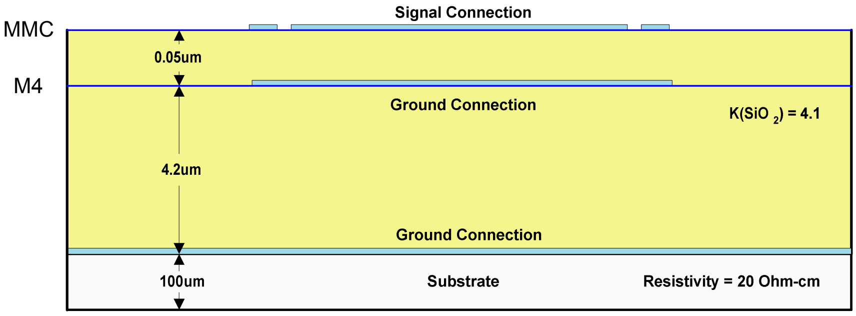

Signal Connection
MMC
0.05um
M4
Ground Connection
K(SiO $_2$) = 4.1
4.2um
Ground Connection
100um
Substrate
Resistivity = 20 Ohm-cm

Figure 3.23 – Momentum Substrate Construction for the Simulation of the Capacitors

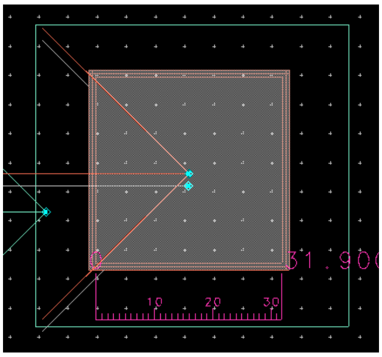


Figure 3.24 – 32µm (0.965pF) Capacitor Momentum Simulation Structure

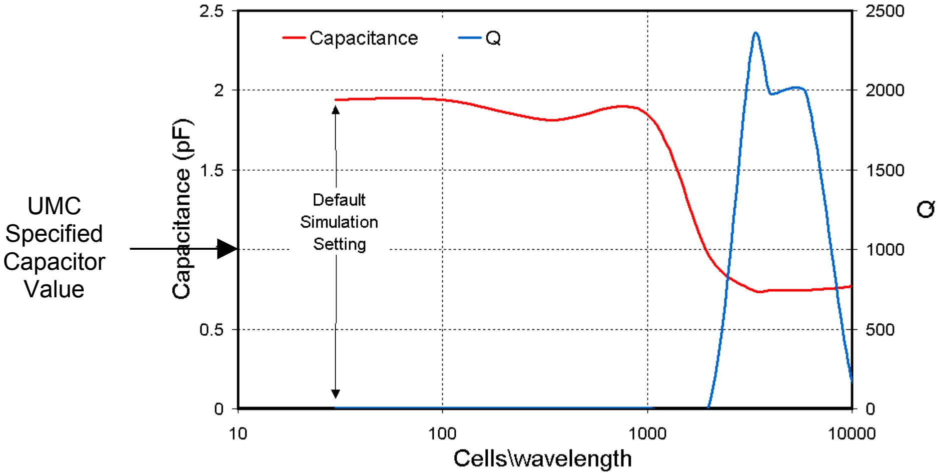


Figure 3.25 – 32µm (0.965pF) Capacitance Simulation results from Momentum with different Mesh Resolutions

These simulation errors are probably caused by the mesh size not being fine enough considering the minimum dimension of the capacitor is 0.05µm. In free-space this distance is equivalent to 3,000,000 cells per wavelength, which will take many hours to simulate and has not been done.

A solution to these ambiguities is to create a test chip to measure the 32µm capacitor. Such a structure was created and can be seen in Figure 3.26. A smaller value of capacitance would lead to greater uncertainty in the measurement, as the bonding PAD would have a greater contribution. The results after de-embedding can be found in section 5.2 on page 63.

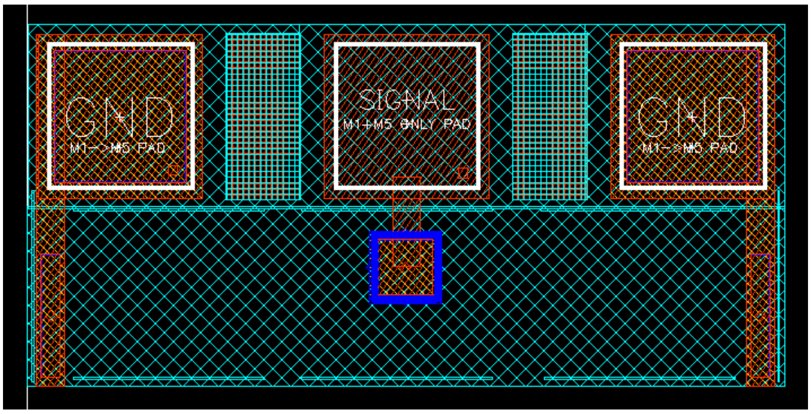


Figure 3.26 – 32µm Capacitor Test Structure

The four newly created capacitors were created as subassemblies in Cadence to allow the same capacitor to be used with confidence in several locations. Normally when a component is created it can be labeled, in this case as a capacitor, such that extraction and LVS (Layout Vs Schematic) can be run in Cadence to give the designer confidence that the circuit layout is correct. Unfortunately, it was found that the capacitors would not extract unless both contacts were on the M5 layer, which is not possible for three out of the four capacitors created. As a result these capacitors were *not* included in the extraction and LVS.

3.3.2 Resistors

Two resistor values are required in the designs: 50-Ohm and 400-Ohm, and these were created because the standard resistor is unacceptably large in size and of a fixed value. The layers are copied and modified from a previous N+Poly resistor design created and tested by a previous PhD student [23].

The 50-Ohm resistor is shown in Figure 3.27 and 3.28. The resistance comes from the central blue-striped poly layer, which normally has low resistance salicide layer on top. The resistance is defined by the width of the poly-layer and the length of the salicide-blocking-layer. The values are calculated by ADS for the resistance required. At either end of the poly-layer there is a connection to the M1 layer and then a series of vias to the M5 layer. All the layers are not shown here in Figure 3.23, and a list of the layers can be found in reference [24].

On either side of the desired resistor there is a poly-layer to stabilize this layer and to give better tolerance. This feature is copied from the standard resistor construction but to reduce the size the width of these is half the width of the resistor.

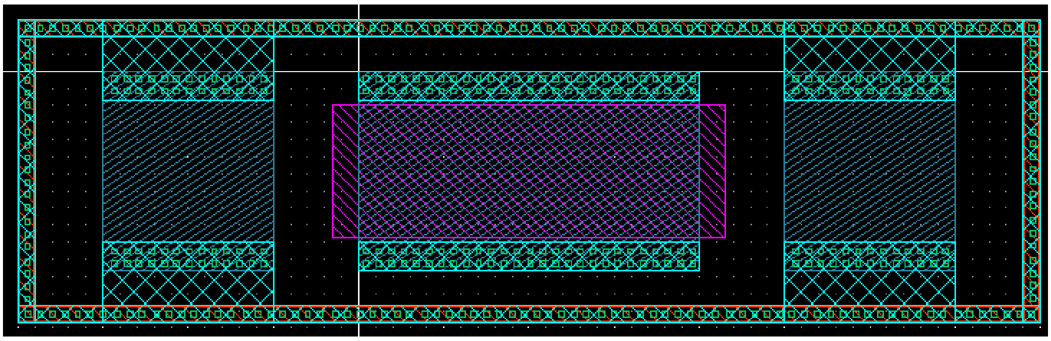


Figure 3.27 – Layout of 50-Ohm Resistor

Figure 3.28 shows the corner detail of the 50-Ohm resistor with other layers enabled. The important feature is to notice is the detail of the guard ring, which is connected to the substrate through the diffusion layer and with contacts as shown by the green squares.

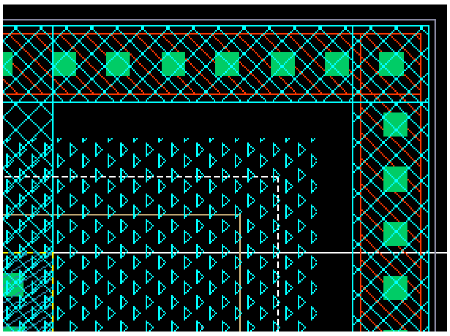


Figure 3.28 – Corner Detail of 50-Ohm resistor

The 400-Ohm resistor is of similar construction and is shown in Figure 3.29. The dimensions are different and the major difference to note is that one end of the poly-layer is tied to ground, as this is required for the circuit construction.

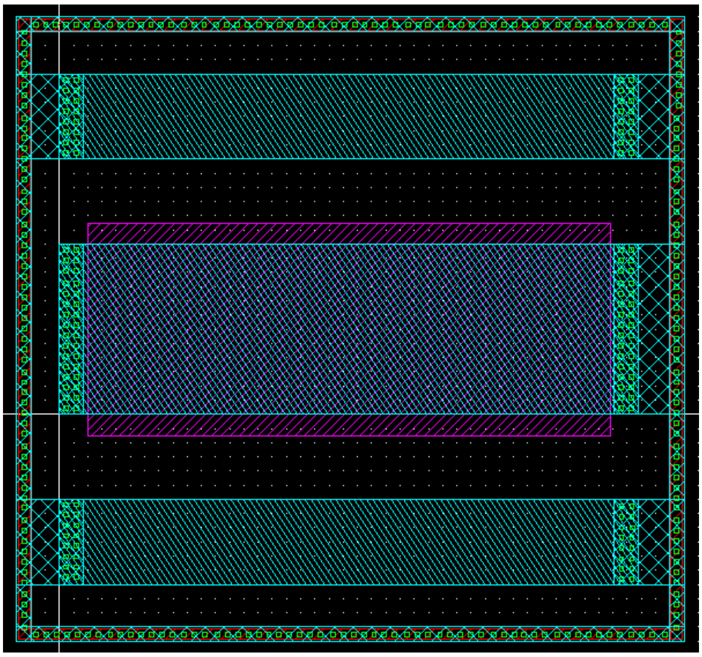


Figure 3.29 – Layout of 400-Ohm Resistor

3.4 Probe Calibrator

A test structure is required to allow the differential probes to be calibrated and is shown in Figure 3.30, and contains both open and short 5-pin pads.

It also has a through connection to allow the losses in the differential probe to be zeroed. This is required because the differential probe is used in an unconventional way with such a test structure not available elsewhere. The through-path track width is 12μm and using the LineCalc tool from ADS with a relative permittivity of 4.1 for SiO_2, a track thickness of 2μm and a height of 6.2μm above the metal-1 plane, the track impedance calculates to be 47.7-Ohm.

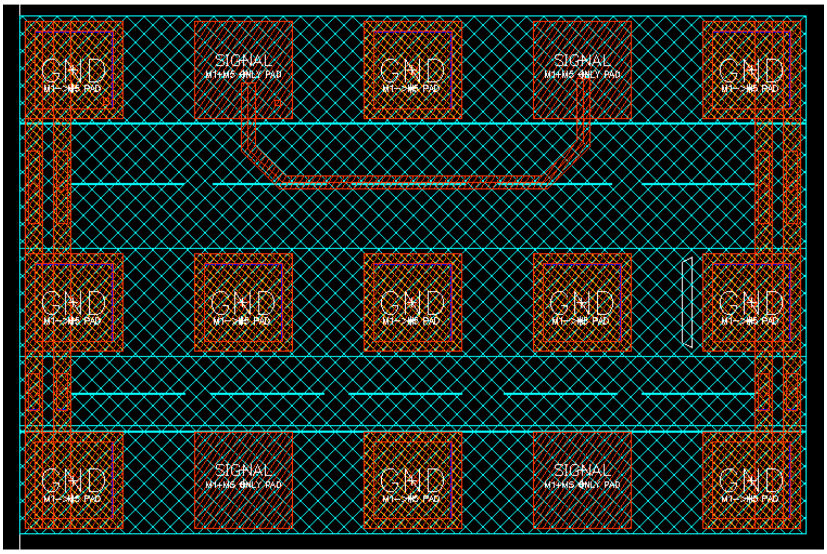

GND
M1->M5 PAD
SIGNAL
M1+M5 ONLY PAD
GND
M1->M5 PAD
SIGNAL
M1+M5 ONLY PAD
GND
M1->M5 PAD
GND
M1->M5 PAD
GND
M1->M5 PAD
GND
M1->M5 PAD
GND
M1->M5 PAD
GND
M1->M5 PAD
GND
M1->M5 PAD
SIGNAL
M1+M5 ONLY PAD
GND
M1->M5 PAD
SIGNAL
M1+M5 ONLY PAD
GND
M1->M5 PAD

Figure 3.30 – Differential Probe Test Structure

4 DESIGN OF THE NORTON AMPLIFIER

This section describes the construction of the complete lossless feedback amplifier.

4.1 General

The complete amplifier design is shown in Figure 4.1, with the area inside the rectangle to be laid down on the IC. The detailed design can be found in sections 3.2.1 and 3.2.3 where the construction of the coupler and the gain block are discussed individually. The separate designs are merged here to form the complete Norton Lossless Feedback Amplifier.

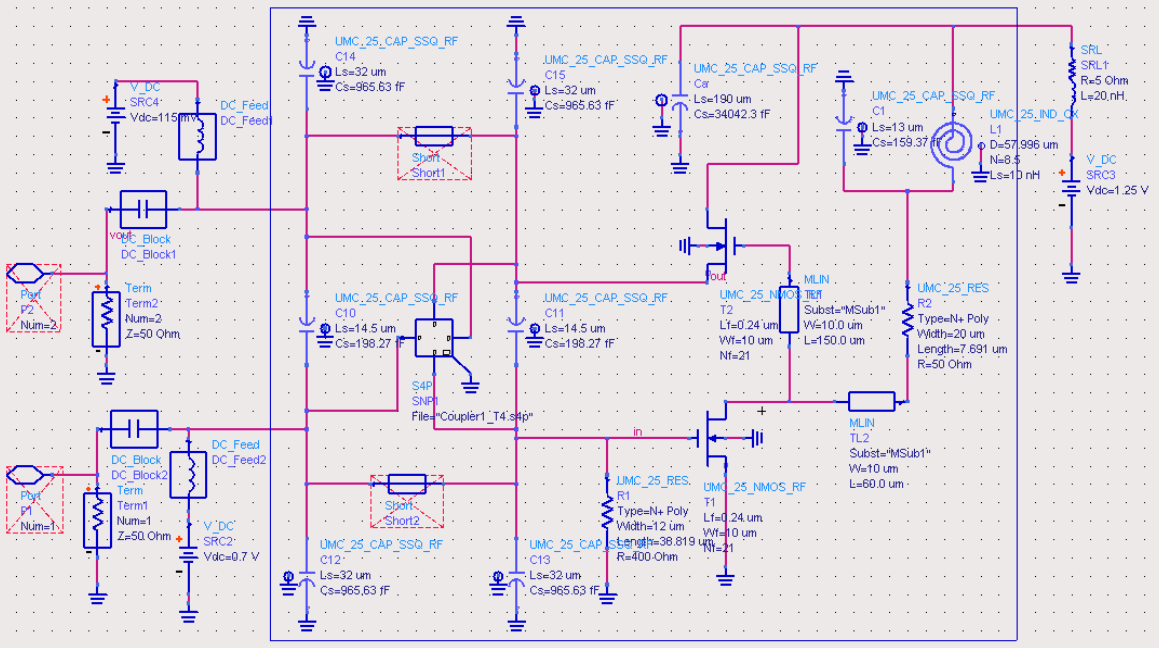

V_DC
SRC4
Vdc=115 mV
DC_Feed
DC_Feed1
vout
DC_Block
DC_Block1
Port
P2
Num=2
Term
Term2
Num=2
Z=50 Ohm
DC_Block
DC_Block2
DC_Feed
DC_Feed2
Port
P1
Num=1
Term
Term1
Num=1
Z=50 Ohm
V_DC
SRC2
Vdc=0.7 V
UMC_25_CAP_SSQ_RF
C14
Ls=32 um
Cs=965.63 fF
UMC_25_CAP_SSQ_RF
C15
Ls=32 um
Cs=965.63 fF
Short
Short1
UMC_25_CAP_SSQ_RF
C10
Ls=14.5 um
Cs=198.27 fF
UMC_25_CAP_SSQ_RF
C11
Ls=14.5 um
Cs=198.27 fF
S4P
SNP1
File="Coupler1_T4.s4p"
Short
Short2
UMC_25_CAP_SSQ_RF
C12
Ls=32 um
Cs=965.63 fF
UMC_25_CAP_SSQ_RF
C13
Ls=32 um
Cs=965.63 fF
UMC_25_CAP_SSQ_RF
Ca
Ls=190 um
Cs=34042.3 fF
UMC_25_CAP_SSQ_RF
C1
Ls=13 um
Cs=159.37 fF
UMC_25_IND_CK
L1
D=57.996 um
N=8.5
Ls=10 nH
SRL
SRL1
R=5 Ohm
L=20 nH
V_DC
SRC3
Vdc=1.25 V
out
UMC_25_NMOS_RF
T2
Lf=0.24 um
Wf=10 um
Nf=21
MLIN
TL1
Subst="MSub1"
W=10.0 um
L=150.0 um
UMC_25_RES
R2
Type=N+ Poly
Width=20 um
Length=7.691 um
R=50 Ohm
in
MLIN
TL2
Subst="MSub1"
W=10 um
L=60.0 um
UMC_25_RES
R1
Type=N+ Poly
Width=12 um
Length=38.819 um
R=400 Ohm
UMC_25_NMOS_RF
T1
Lf=0.24 um
Wf=10 um
Nf=21

Figure 4.1 – Schematic of Integrated Norton Amplifier. The Amplifier Circuit laid out on the IC is shown inside the rectangle.

The simulations show the current consumption to be 3.47mA through T1 and 9.26mA through T2, which with a supply voltage of 1.25V gives a power consumption of 15.9mW. The basic performance measures are shown in Figure 4.2.

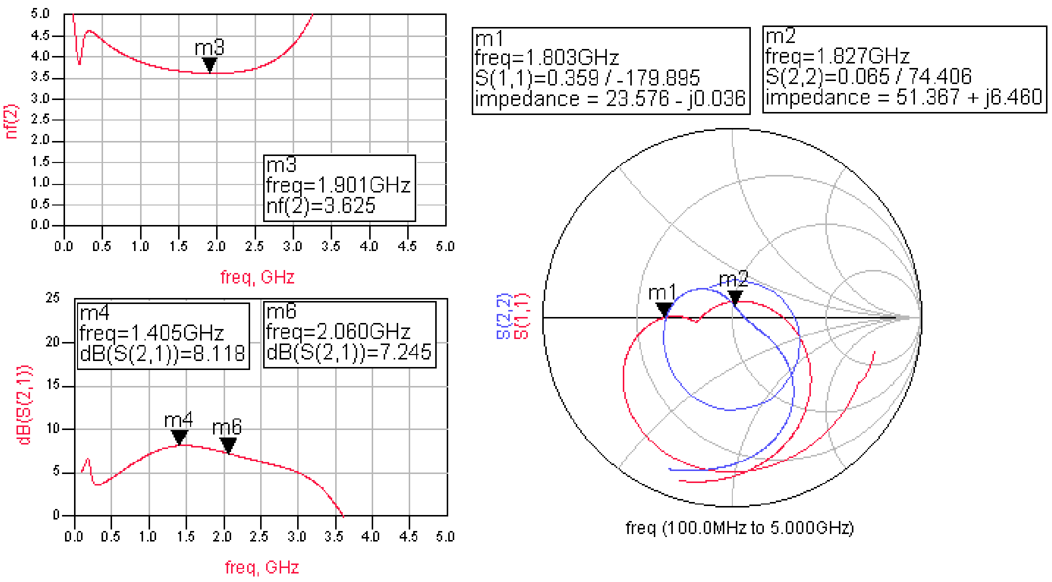


Figure 4.2 – Basic Performance measures of Integrated Norton Amplifier

The Noise Figure is 3.6dB and remains less than 4dB from 1GHz to 2.7GHz. The gain of the amplifier from 1.5 to 2GHz varies from 8.1dB to 7.25dB with both the input and output impedances acceptable but with the input impedance having the worst mismatch. This is a consequence of matching to the high input impedance of the input FET.

4.1.1 Stability and Component Tolerance

All measures of amplifier stability are shown in Figure 4.3. These show the amplifier to be close to being unconditionally stable, with a small region of load impedance at the top of the Smith chart likely to cause the amplifier to become unstable. This is a good result as such impedance is unlikely to occur. Furthermore, if the amplifier is to be used as a front-end amplifier, the input impedance of the following stage can be designed such that it will not present these impedances at the frequencies concerned.

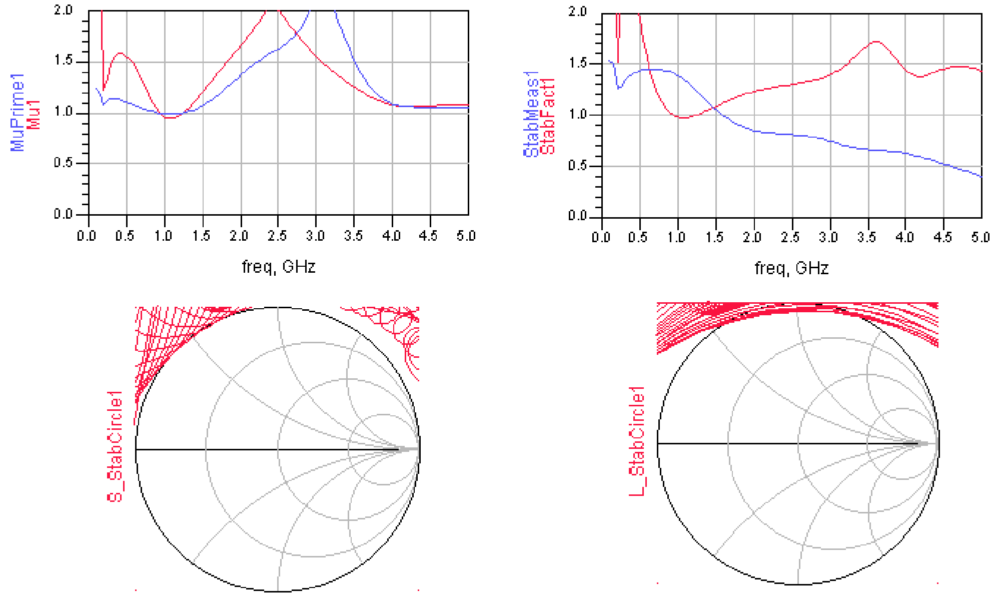


Figure 4.3 – Measures of Amplifier Stability

Some effort was made to simulate the affects of process variation on the stability and gain of the amplifier. The 400-Ohm resistor (R1) was added in the design to the gate of the bottom FET in order to improve the amplifier stability and hence it is important to consider the affect of variation on this component.

It is known from design rules that the largest variation is in the fabrication of the resistors [83], which for the N+ poly sheet resistance can vary from a minimum of 80-Ohm/sq and a maximum 180-Ohm/sq. Stability is measured with a wider tolerance than this from 0.5R to 1.5R to ensure compliance, and both resistors used in the design (400-Ohm and 50-Ohm) are varied in the same way with the μ and μ’ measures shown in Figure 4.4.

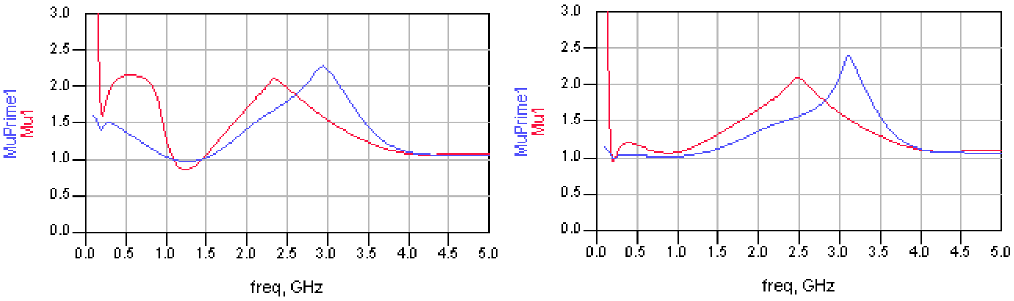


Figure 4.4 – Stability of Amplifier with Change in Resistance. Left 0.5R; Right 1.5R.

The amplifier can be seen to be slightly less stable when the resistance values are halved, but the amplifier should remain stable enough to be tested.

In addition, plots of the variation in gain are made in much the same way by varying the two resistors and the results can be seen in Figure 4.5. The gain drops by about 0.7dB between the two extremes of resistance and it can be seen that the frequency response changes.

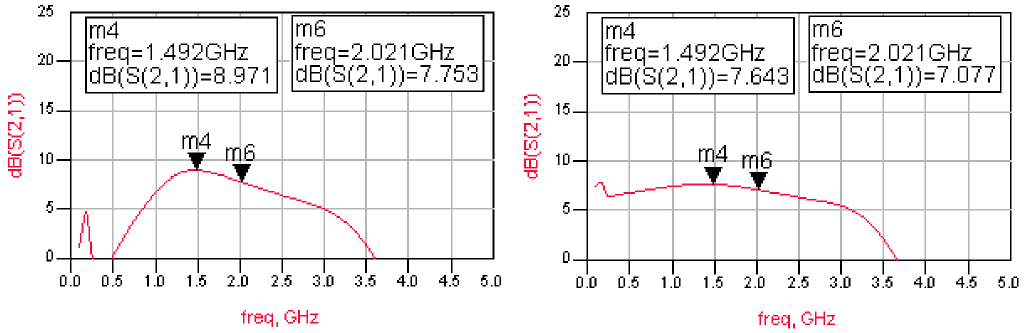


Figure 4.5 – Gain of Amplifier with Change in Resistance. Left 0.5R; Right 1.5R.

4.1.2 Linearity

An important motivation behind this amplifier topology is the high linearity that can be achieved from low voltage power supply. The output 1dB compression point does not improve much; it is simulated to be 4.37dBm and shown in Figure 4.6. The output phase can has an error of 1° when the output power is 5.93dBm.

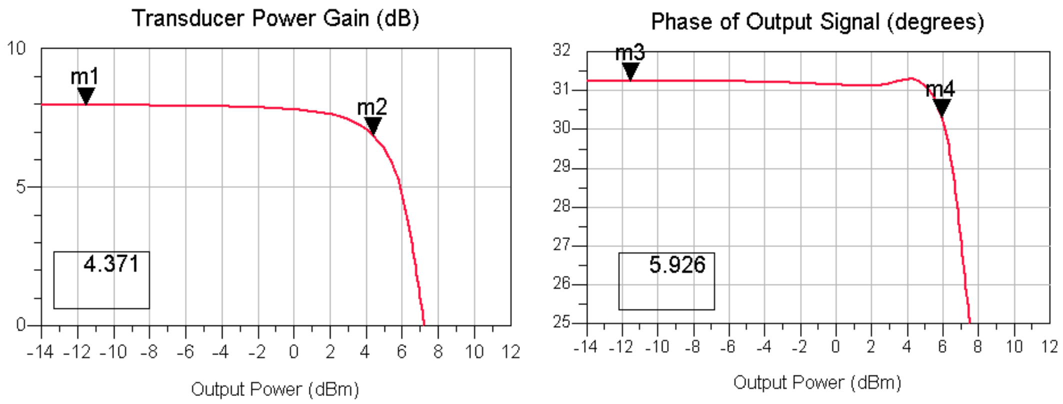


Figure 4.6 – 1dB point and Phase-Power of Lossless Feedback Amplifier

The main measure of linearity is IIP3 and the variation of this with frequency is shown in Figure 4.7, with the increase compared to the amplifier without feedback shown in Figure 4.8. The IIP3 is high for this supply voltage & power consumption at greater than 16dBm over the frequency band from 1.5GHz to 2GHz and showing a minimum of 10dB improvement across this band.

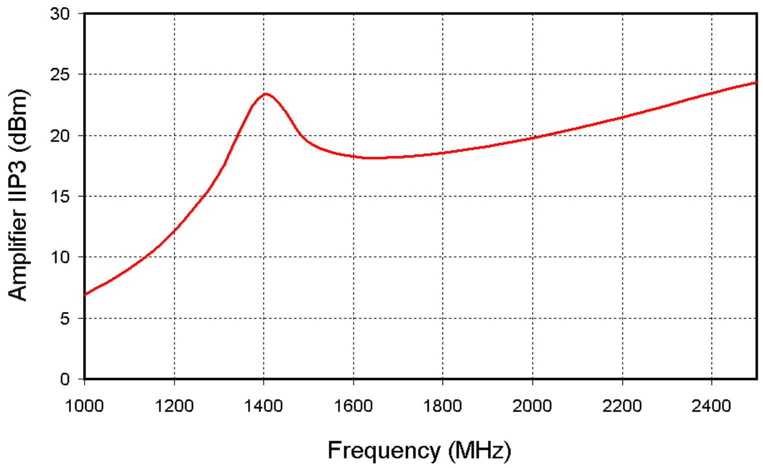


Figure 4.7 – IIP3 of Norton Amplifier

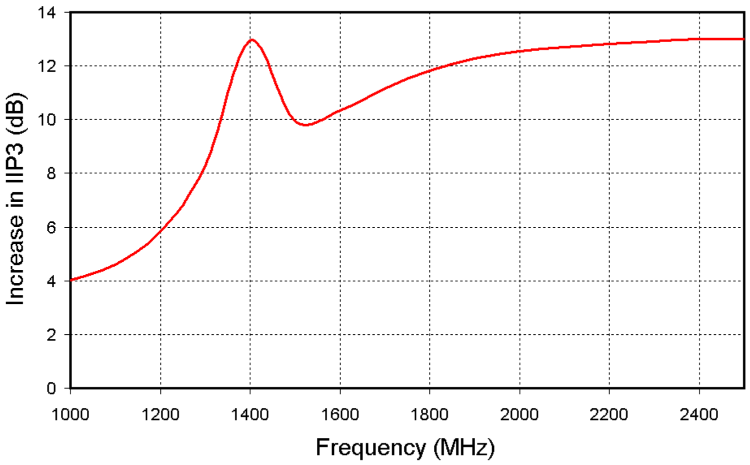


Figure 4.8 – Improvement in IIP3 of Norton Amplifier compared to Gain-Block

4.1.3 Layout

The amplifier layout can be seen in Figure 4.9. The layout of the coupler and gain-block are described individually in sections 3.2.1 (Figure 3.8) and 3.2.3 (Figure 3.18). The amplifier is laid out between two 5-pin pads, with the pad on the left for the input and output RF signals, the input signal is on the lower of two signal pads. The 5-pin pad on the right allows 1.25V to be connected to the amplifier on the top signal pad and with this monitored as a sense connection using the bottom pad.

The power supply in decoupled with 36pF of capacitance (Ca) placed above and close to the spiral inductor. A schematic of the amplifier was drawn in Cadence and the amplifier passed both the DRC and the LVS checks in comparison to the schematic. The LVS check was not optimum as none of the capacitors nor the inductors used in the coupler could be extracted for LVS.

An earth plane is created on the M1 layer and some effort was made to break this into smaller sections to comply with a DRC rule specifying the maximum dimension. The circuit fails this DRC check but this was not considered serious enough to prevent fabrication. In addition a number of contact connections were placed from the M1 layer to the substrate to improve the ground connection.

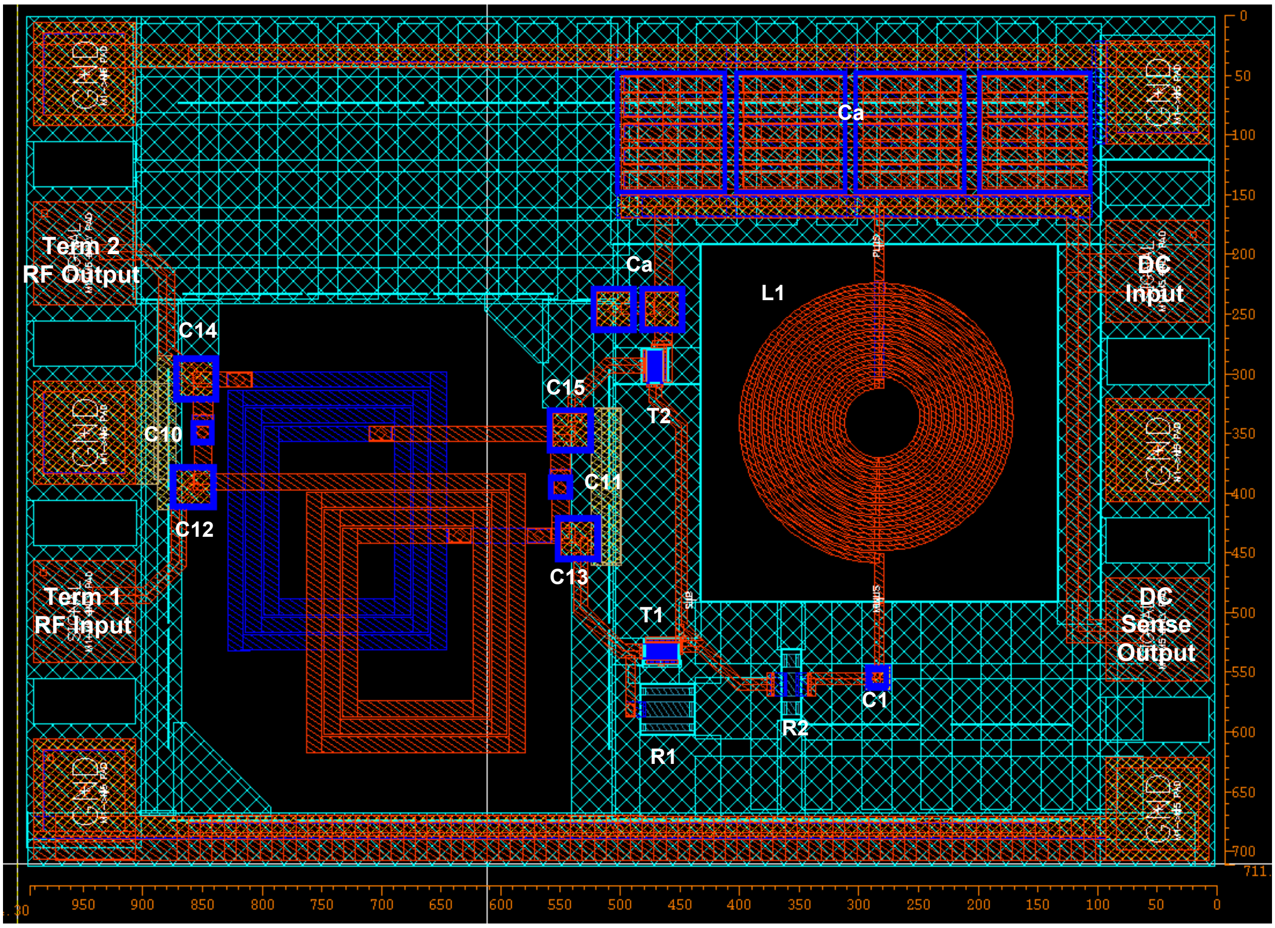

Ca
Term 2
RF Output
Ca
L1
DC
Input
C14
C15
T2
C10
C11
C12
C13
Term 1
RF Input
T1
DC
Sense
Output
C1
R2
R1
GND
GND
GND
GND
GND
0
50
100
150
200
250
300
350
400
450
500
550
600
650
700
711
30
950
900
850
800
750
700
650
600
550
500
450
400
350
300
250
200
150
100
50
0

Figure 4.9 – Amplifier IC Layout

5 TEST RESULTS

5.1 Analysis of Fabricated IC

It is necessary to start by analyzing the returned IC for differences from the nominal values that were used in the original simulations. Three differences have been found, two of which are serious and have a major impact on the IC performance.

5.1.1 Metal Layer Conductivity

Probably the least significant of the deviations, is the conductivity of the metals layers although this does have an influence on the performance of the RF directional couplers. Simulations using the Discrete Component Coupler S-parameter file shown in Figure 5.1 indicate that the resistance of the winding on the top metal-5 layer should be 3.61-Ohm and the resistance of the winding on the metal-4 layer should be 8.55-Ohm. The resistance of four devices was measured and averaged to be 2.82-Ohm for the metal layer-5 and 9.81-Ohm for metal layer-4.

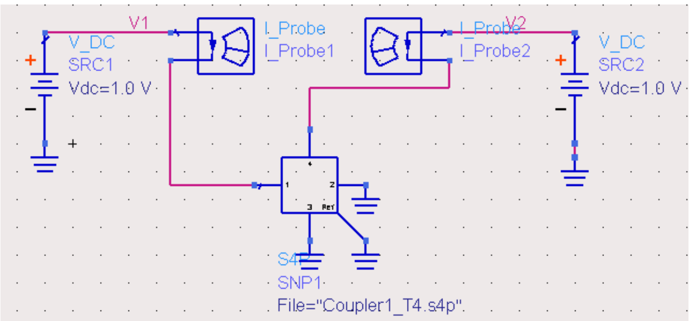


Figure 5.1 – Resistivity Measurement Simulation for the Discrete Component Coupler Shown in Figure 3.4 on page 39.

These results can be used to find the resistivity of the metal layers by estimating the conductivity values in Momentum and comparing the resulting S-parameter file with the ADS simulation circuit shown in Figure 5.1. After several iterations the resistivity of the metal layers was found to be 0.0178 Ohm/sq for M5, and 0.0625 Ohm/sq for M4.

The maximum and minimum limits for the M5-metal layer are defined by the supplier to be between 0.010 to 0.030 Ohm/sq. The conductivity of the metal-5 layer at 0.0178 Ohm/sq is within specification and is slightly better than the nominal value used in the simulations.

In a similar way, the maximum and minimum limits for M4-metal layer are defined by the supplier to be between 0.035 to 0.075 Ohm/sq. The conductivity of the metal-4 layer at 0.0625 Ohm/sq is within specification and is worse than the nominal value used in the simulations.

5.1.2 Transconductance

A major problem with the returned IC was found to be the transconductance of the transistors. This was measured on the gain-block TR1 transistor using the LabView virtual instrument 'Plot_Id-Vg.vi' described in Appendix B on page 99. The curves plotted are shown in Figure 5.2 and show how the drain-current of this transistor changes with the gate-voltage for four delivered IC's and included on this graph is the ADS simulation results and the test results for a 20-finger FET from a previous fabrication.

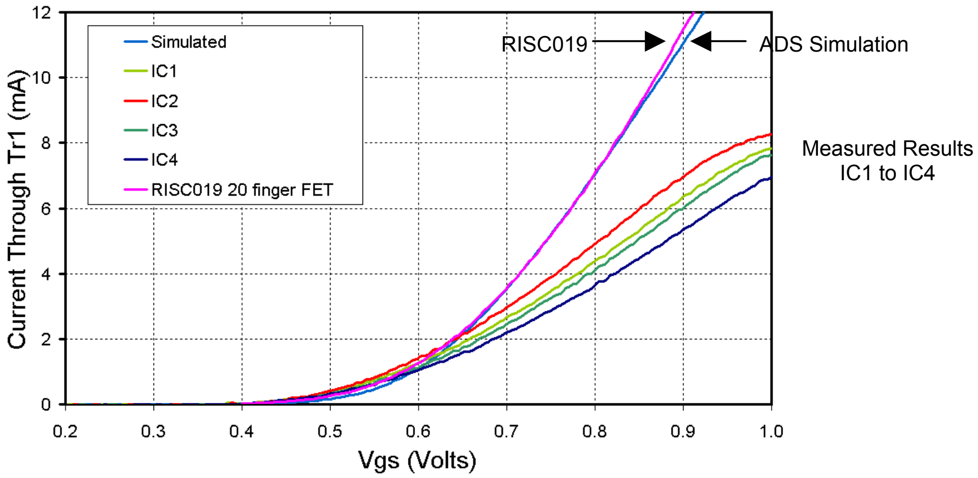


Figure 5.2 – Plot of Id against Vg for transistor TR1 and with Vd=1.25V. This graph shows both the simulated and measured values as well as measured results for a 20 finger FET using the same process.

It can be seen that there is a striking difference between the measured and simulated results indicating that either some fault has occurred in the fabrication process or there is a fault in the design or measurement. The transistors used in the design were unmodified from the standard cell. As a consequence of these measurements, some discussion was made with the supplier about this problem and UMC has admitted to an error in the N+ layer in the fabrication [26]. UMC has agreed to rebuild the batch, but this is too late for the delivery of this Thesis.

Figure 5.3 is a clearer plot of how the gm is affected and is plotted here for the average of the four transistors tested and also from the ADS simulation results. The gm of the transistors can be seen to be approximately half that expected. In addition, the four transistors show a spread of nearly 20% in the current flow for a given gate voltage. This spread is much higher than expected and is in itself an indication of a serious problem, however the low transconductance is the main problem and will present a problem with further amplifier testing.

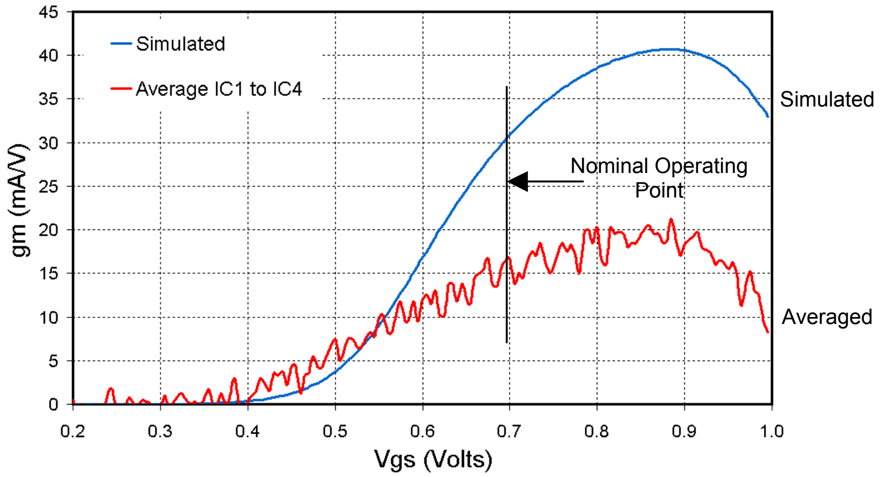


Figure 5.3 – Plot of transistor transconductance (gm) against Vgs, for the Simulated and Tested transistors.

In order to continue with the testing of the amplifier and to get some meaningful results, it is necessary to try to recover this gm by biasing the amplifier at a higher voltage and current. From Figure 5.3 and at the design value for Vg of 0.7V, the transistor can be seen to have a gm of 30 mA/V. Similar sets of plots were made with a drain-voltage of 3.3V and these results are shown in Figure 5.4. This graph shows that the gm can be mostly recovered with a drain current that is approximately 3 times higher than the designed current, and a gate voltage of 1V. To allow further testing of the amplifier, the input transistor is biased with a gate voltage of approximately

1V and a drain current of 11mA. The drain current of output transistor is also increased, the design current is 9.45mA and this is increased to 30mA for testing.

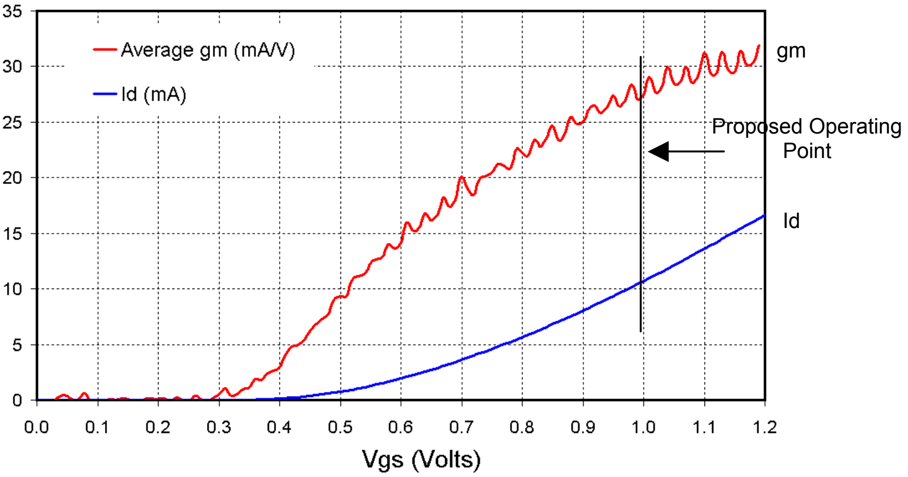


Figure 5.4 – Plot of transistor transconductance (gm) and Id against Vgs, at Vd=3.3V to select new bias point.

5.1.3 PolySilicon Resistors

The 400-Ohm resistor on the input to the gain-block is designed as an N+ Poly resistor, of which the structure is copied from a previously tested design [23]. The N+Poly structure is specified by the supplier to have a (min, typ, max) sheet resistance of (80, 130, 180)-Ohm/sq. Four devices were tested and measured to be 688-Ohm and these were observed to have a low spread of values of less than 20-Ohm.

This resistance corresponds to a sheet resistance of 224-Ohm/sq, which is well outside the range specified by the supplier. This can also be associated with the N+ error that UMC have admitted to [26].

5.2 32µm Capacitor

One of the test structures fabricated is a 32µm capacitor that was constructed such that the lower plate of the capacitor is connected directly to the earth plane layer on metal-1 with a large number of vias. This 32µm capacitor on ten IC's was measured and de-embedded using the University Matlab deembedding scripts [29] and found to be 1.0321pF, and with a tight spread of values shown by a standard deviation of 0.0171pF. At the same time the series resistance was measured to be 0.0172-Ohms. A link to the data can be found in Appendix D.

The capacitor construction described in section 3.3.1 should according to the UMC process produce a capacitance of 0.965pF and have a series resistance on 0.27-Ohm [ref 15 table 4.1]. As a consequence the measured capacitance is in error by +6.8%; however this variation is within the tolerances specified by UMC [15] that specifies the distance from the MMC to M4 layers to be between 0.045 to 0.055µm implying a ±10% tolerance in capacitance value should be expected.

The series resistance is however much lower than that specified by the standard capacitor model and this may be a result of the capacitor construction where the bottom plate of the capacitor is connected directly to metal-1 through a large number of vias on the intermediate metal layers. However at this resistance value it is difficult to know for sure if this is a measurement error, especially as the resistance has a large standard deviation of 0.167-Ohm. However, with a mean resistance value that is less than a fifteenth of that specified, the result looks promising.

5.3 Discrete Component Coupler

The measured and simulated results for the discrete component coupler are shown in Figure 5.6 with a diagram of the coupler reminding the reader of the port definitions shown in Figure 5.5. It can be seen that the simulated and measured results are similar, but are not exact.

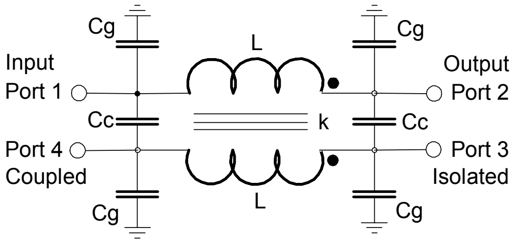


Figure 5.5 – Discrete Component Coupler

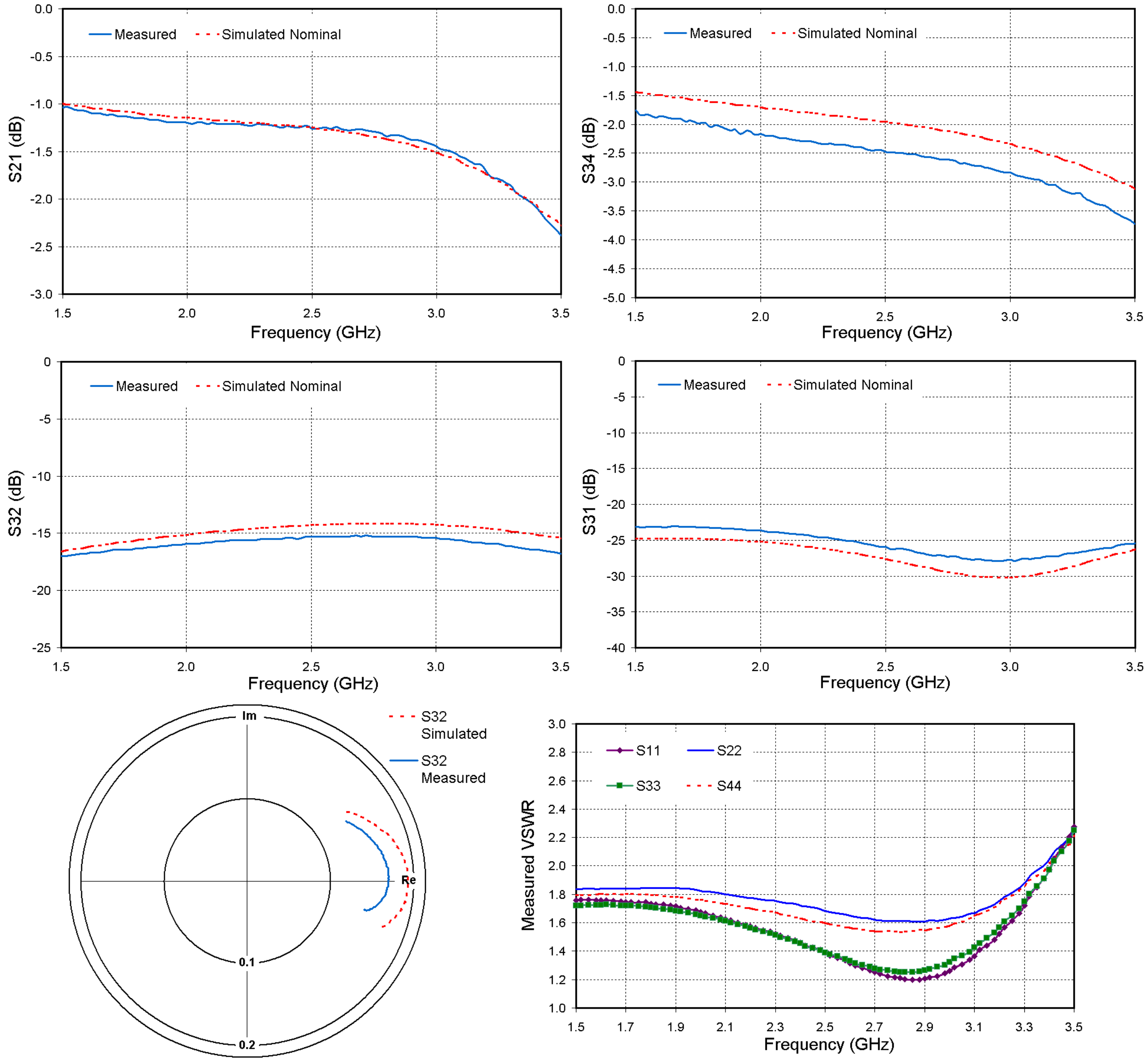


Figure 5.6 – Comparison of Simulated and Measured results For the Discrete Component Coupler using Nominal Semiconductor Values

The forward path loss S21 is very similar to the simulated results giving 1.2dB of loss at 2.5GHz. The isolated port S31 is approximately –25dB and is 2dB worse than the simulated results. The coupling level S32 and the phase of this which is important for the correct operation of the amplifier, are in reasonably close agreement with the simulated results showing an extra 1dB of loss and with a phase response that has 6-degrees of error at the center frequency of 2.5GHz. At 1.8 GHz the phase-lead is 23.6-degrees whereas the simulated results shown in Figure 3.7 on page 41 show 27.4-degrees.

The simulated results were carried out using nominal resistivity values for the metal layers and with 6.2µm from the bottom of M4-layer to the substrate. The biggest difference between the simulated and measured results is S34 where the losses at 2.5GHz are simulated at 1.8dB and measured to be 2.5dB.

A second simulation was made using the conductivity values derived for the metal layers from section 5.1.1 above and this goes some way to explain the difference in performance between the simulated and measured results. However there remained a difference and a better correlation was found when the distance to the substrate is reduced to 4.4µm. The measured and simulated results under these conditions for S34 are shown in Figure 5.7. Despite these corrections there remains a difference between the measured and simulated results that cannot be explained.

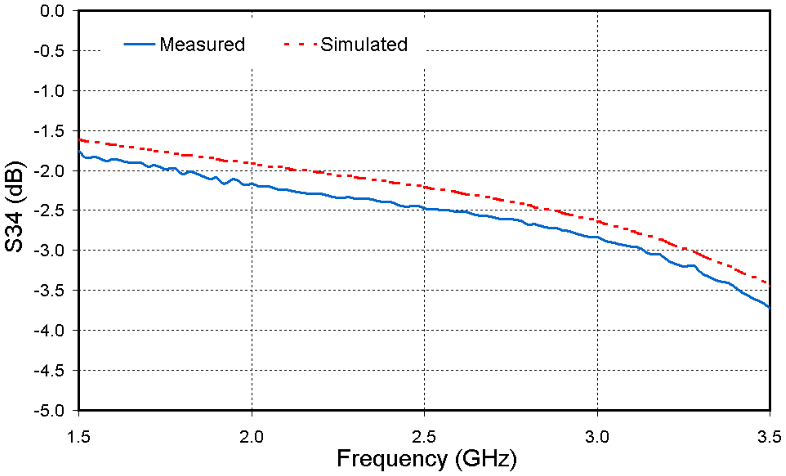


Figure 5.7 – S34 for the Discrete Component Coupler using Modified values for resistivity and 4.4µm of the M4 layer above the substrate.

The theory behind reducing the oxide layer in this way is because metal-1, 2 and 3 are not part of the coupler construction, and the dummy pattern that was required to maintain flatness on the IC was blocked from forming as part of the coupler design. The dimension from the M4 layer to the substrate is given in ref [16] to be 6.2µm typical. This same document gives the typical thickness of the metal layers to be 0.6µm and hence with these layers blocked the oxide thickness can be taken to be 4.4µm.

A paper describing the construction and results of this coupler has been written and submitted, as this is the first time to the author's knowledge that such a circuit has been designed and built on a CMOS substrate [25].

5.4 Transformer Coupler

The measured and simulated results for the transformer coupler are shown in Figure 5.9 with a diagram of the coupler reminding the reader of the port definitions shown in Figure 5.8. It can be seen that the simulated and measured results are very different.

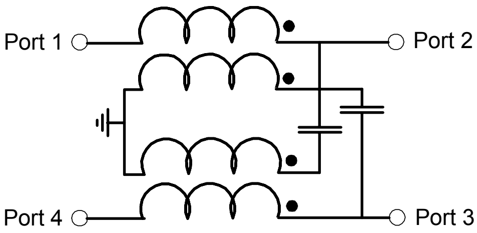


Figure 5.8– Transformer Coupler

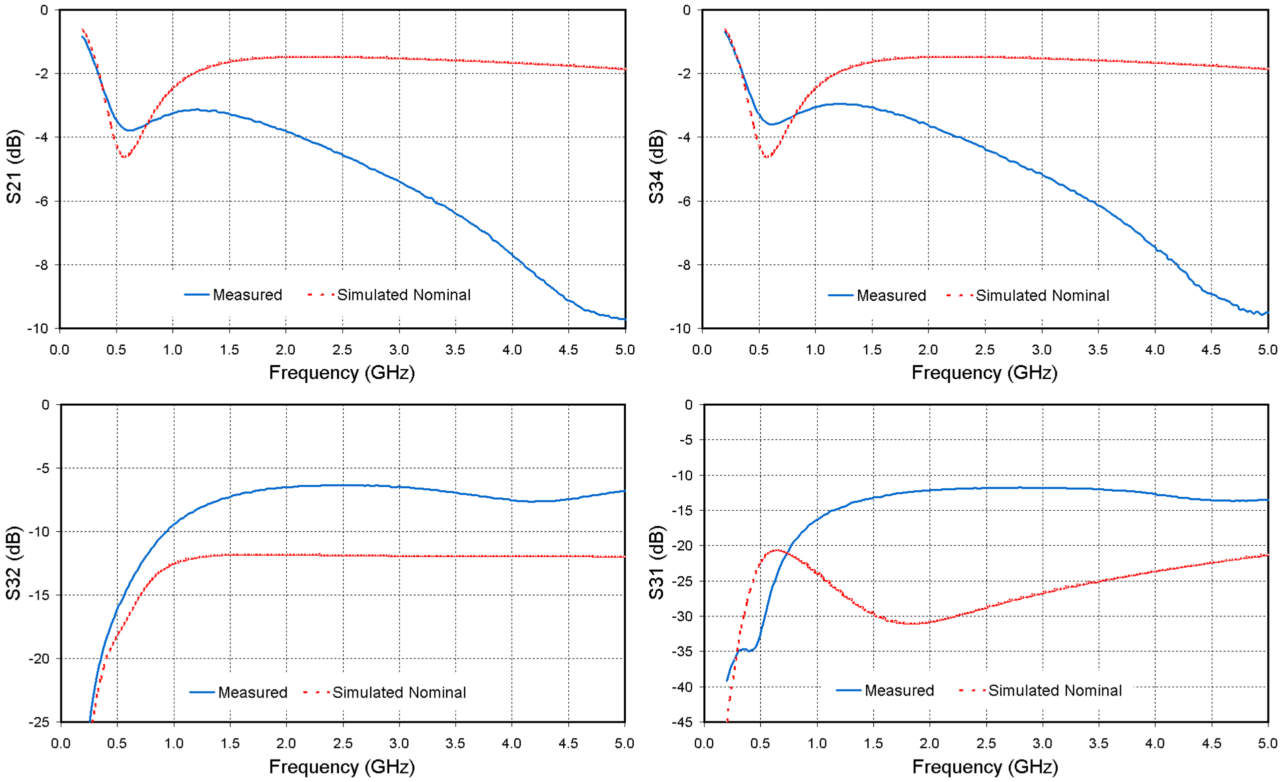


Figure 5.9 – Comparison of Simulated and Measured results for the Transformer Coupler using Nominal Values

In an effort to get a better understanding of these differences three changes were made to the simulation circuit and these are shown in Figure 5.10. The first change is the transformer was re-simulated with an oxide thickness of 4.4µm and with the metal resistivity values as suggested in the previous chapter. This was found to have only a small affect on the simulation results.

The second change was to model the thin track between the capacitor and the output connection of dimension 10µm by 250µm, as simulations showed that if this track has a large resistance then this would affect the results in the way observed. The Momentum simulation results for this track implied a series resistance of 1.25-Ohm plus a small inductance, and this resistance was checked by measurement to be 1.36-Ohms. However when the 2-port s-parameter file is included in the simulation, the affect is small.

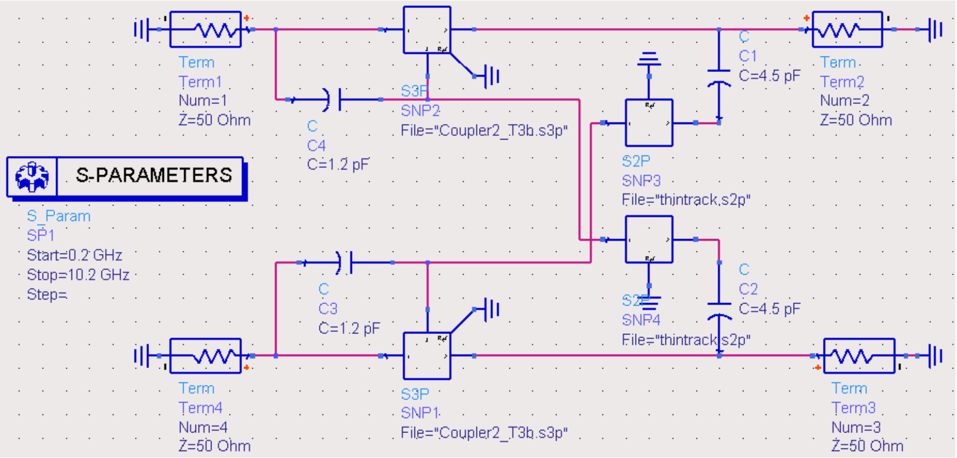

Term
Term1
Num=1
Z=50 Ohm
C
C4
C=1.2 pF
S3P
SNP2
File="Coupler2_T3b.s3p"
S-PARAMETERS
S_Param
SP1
Start=0.2 GHz
Stop=10.2 GHz
Step=
S2P
SNP3
File="thintrack.s2p"
C
C1
C=4.5 pF
Term
Term2
Num=2
Z=50 Ohm
C
C3
C=1.2 pF
S2P
SNP4
File="thintrack.s2p"
C
C2
C=4.5 pF
Term
Term4
Num=4
Z=50 Ohm
S3P
SNP1
File="Coupler2_T3b.s3p"
Term
Term3
Num=3
Z=50 Ohm

Figure 5.10 – Comparison of Simulated and Measured results for the Transformer Coupler with Additional Losses.

The third and final change to the simulation circuit is with the addition of a 1.2pF capacitance between the windings, shown in Figure 5.10 by the addition of capacitors C3 and C4. With this and the other changes, the simulated and measured results are now in much closer agreement and these can be seen in Figure 5.11.

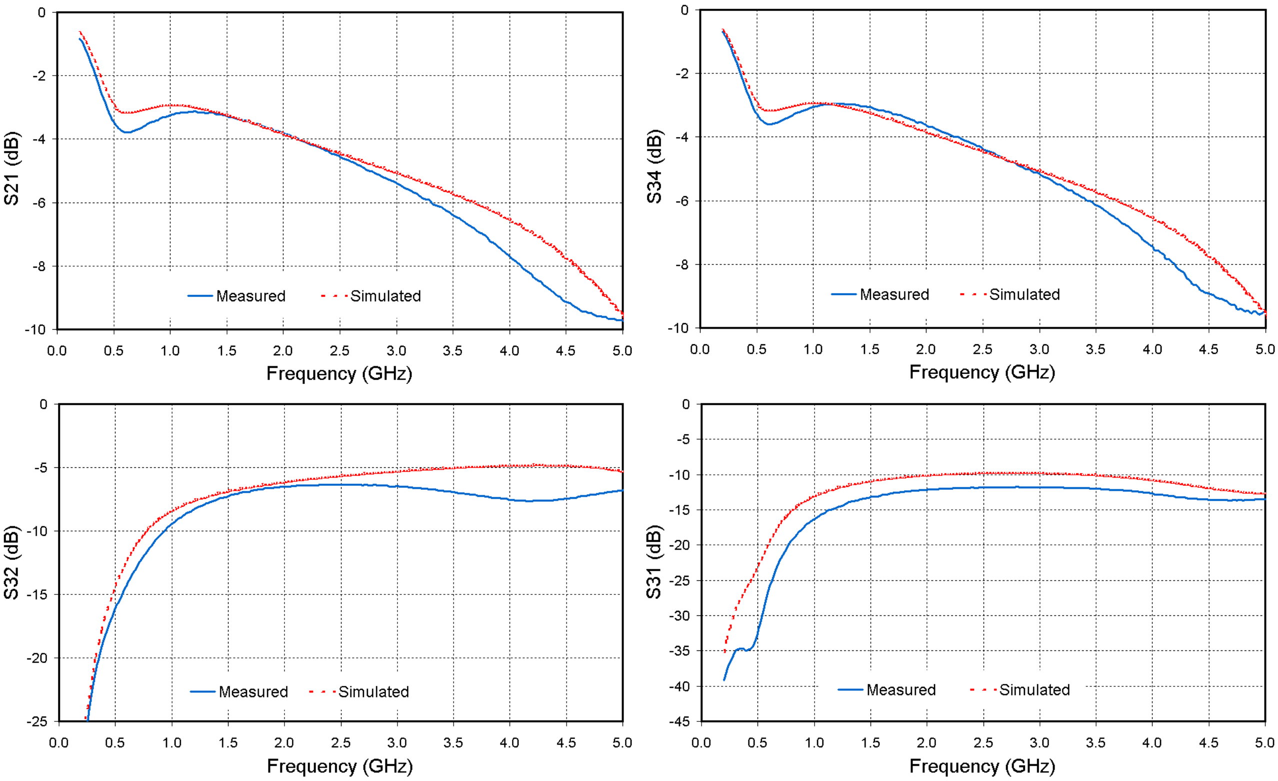


Figure 5.11 – Comparison of Simulated and Measured results for the Transformer Coupler with Additional Losses

This extra capacitance is added after the inter-winding capacitance was measured to be 1.6pF. This was done after the thin tracks out of the 4.5pF capacitors on one of the transformer couplers was cut courtesy of RFMD. The inter-winding capacitance was then measured between 50 and 200MHz to be 1.6pF.

In addition an ADS simulation was set up as shown in Figure 5.12 to measure the inter-winding capacitance of the simulated transformer. A low frequency signal of 1Vpp drives a series capacitor, which then connects to the top metal winding of the 2-port simulation. The capacitor C1 is adjusted to achieve 0.5Vpp at *vacout*, thereby equaling the inter-winding capacitance and giving a value of 0.4pF.

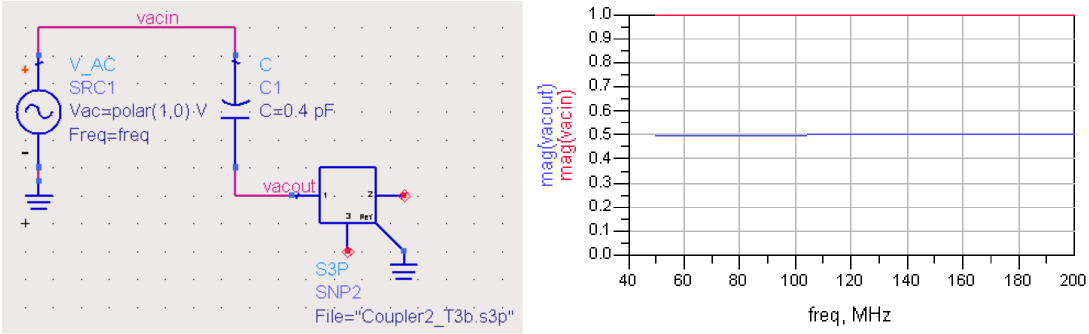


Figure 5.12– Capacitance measure of Simulated Transformer Winding

As a consequence the 2-port S-parameter file for the coupler transformer shows a shortfall of 1.2pF in the interwinding capacitance such that when 1.2pF is added to the simulation circuit the measured and simulated results are in reasonably close agreement.

To check that the interwinding capacitance is a reasonable estimate, a MathCAD sheet is written and found on page 95, where the capacitance is calculated according to the simple capacitance equation and this sheet produces a capacitance value of 1.6pF. The conclusion that can be drawn from this is that Momentum does not calculate accurately the capacitance value of a parallel plate capacitor, with a simple math's equation producing a much more accurate result. This is a conclusion mirrored from Section 3.3.1 where Momentum was used to simulate the standard UMC capacitor but also produced inaccurate results.

An attempt was made to increase the mesh resolution in the Momentum simulation from a setting of 400 cells/wavelength at 10GHz to a finer resolution to verify if this is the cause of the inaccuracy, but the simulation fails.

5.5 Amplifier

5.5.1 Amplifier Simulation

The final and most important circuit-blocks to be investigated are the Amplifier and the Gain-block. To obtain the performance in these circuits that will allow some comparison to the original simulations and to compensate for the poor transconductance of the transistors, the circuits by re-biased to work at a Vd of 3.3V and with a drain current that is three times greater than the original simulations.

Furthermore, in an attempt to obtain a comparison between the measured and simulated results, simulations are made on both the gain-block and the amplifier with the values for Vd, resistance and gm estimated for the supplied IC. The transistor is modeled with a reduced gm by halving the number of fingers from 21 to 11. This of course is an approximation but may allow some comparison in analyzing the results. The schematic for the 'bad' amplifier is shown in Figure 5.13, but unfortunately it was found that the only performance characteristic where both the measured and simulated results are close agreement is the amplifier gain and this is shown in Figure 5.14.

Nevertheless it is possible to proceed with testing and to show the difference in performance between the gain-block and the amplifier.

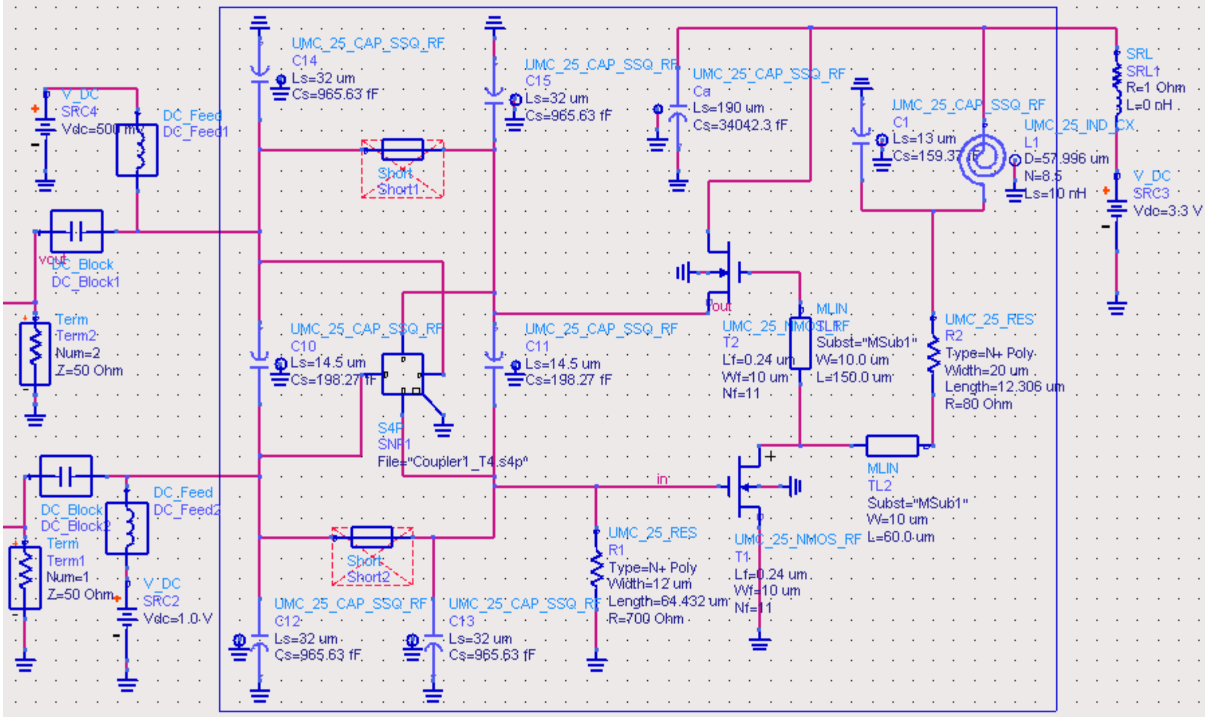

V_DC
SRC4
Vdc=500 mV
DC_Feed
DC_Feed1
DC_Block
DC_Block1
vout
Term
Term2
Num=2
Z=50 Ohm
UMC_25_CAP_SSQ_RF
C14
Ls=32 um
Cs=965.63 fF
UMC_25_CAP_SSQ_RF
C15
Ls=32 um
Cs=965.63 fF
Short
Short1
UMC_25_CAP_SSQ_RF
Ca
Ls=190 um
Cs=34042.3 fF
UMC_25_CAP_SSQ_RF
C1
Ls=13 um
Cs=159.37 fF
UMC_25_IND_CX
L1
D=57.996 um
N=8.5
Ls=10 nH
SRL
SRL1
R=1 Ohm
L=0 nH
V_DC
SRC3
Vdc=3.3 V
UMC_25_CAP_SSQ_RF
C10
Ls=14.5 um
Cs=198.27 fF
UMC_25_CAP_SSQ_RF
C11
Ls=14.5 um
Cs=198.27 fF
S4P
SNP1
File="Coupler1_T4.s4p"
out
UMC_25_NMOS_RF
T2
Lf=0.24 um
Wf=10 um
Nf=11
MLIN
TL1
Subst="MSub1"
W=10.0 um
L=150.0 um
UMC_25_RES
R2
Type=N+ Poly
Width=20 um
Length=12.306 um
R=80 Ohm
DC_Block
DC_Block2
DC_Feed
DC_Feed2
Term
Term1
Num=1
Z=50 Ohm
V_DC
SRC2
Vdc=1.0 V
Short
Short2
in
MLIN
TL2
Subst="MSub1"
W=10 um
L=60.0 um
UMC_25_RES
R1
Type=N+ Poly
Width=12 um
Length=64.432 um
R=700 Ohm
UMC_25_NMOS_RF
T1
Lf=0.24 um
Wf=10 um
Nf=11
UMC_25_CAP_SSQ_RF
C12
Ls=32 um
Cs=965.63 fF
UMC_25_CAP_SSQ_RF
C13
Ls=32 um
Cs=965.63 fF

Figure 5.13 – Schematic of the 'bad' Integrated Norton Amplifier with modified gm and Resistance to reflect the measured values.

5.5.2 Amplifier Results

The frequency response of the gain-block and amplifier with the increased drain current are shown in Figure 5.14. The response of the gain-block peaks with a gain of 16.5dB at 1.8GHz and shows that the design of the resonance circuit is as expected and is close to the original simulations presented in section 3.2.3 where it peaks at 1.73GHz and with 17dB of gain. Not only does this show that the layout of the resonant circuit is acceptable but it also shows that the transconductance increase is acceptable for further testing.

The test results presented here were measured using a number of specifically written LabVIEW test scripts where the bias voltage and current to both the amplifier and gain-block were provided using two designs of PCB. The information about these can be found in Appendix B on page 97 along with diagrams of test setups.

The amplifier was measured to have a gain at 7.9dB over the frequency range from 1.5GHz to 2GHz and this has some agreement with the simulation results from the 'bad' amplifier in Figure 5.13. The original simulation from Section 4.1 on page 55 give a gain of between 8.1dB and 7.2dB for the simulated amplifier over this range.

The noise-figure of the gain-block and amplifier are shown in Figure 5.15. The absolute value for the noise-figure is again difficult to quantify, however the increased noise between the amplifier and gain-block is as expected, and can be explained by the losses on the input signal path of the directional coupler. These losses are shown as the measured S21 value in Figure 5.6 at 1.2dB. The result in Figure 5.15 shows an unexpected ripple that is usually associated with a component impedance miss-match. The cause of this ripple is unknown and is not visible when the gain is measured using the NF meter.

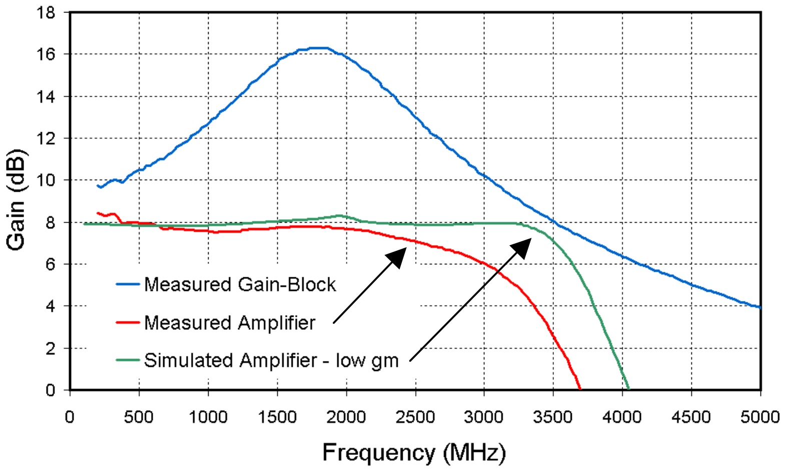


Figure 5.14 – Gain of Gain-Block and Amplifier

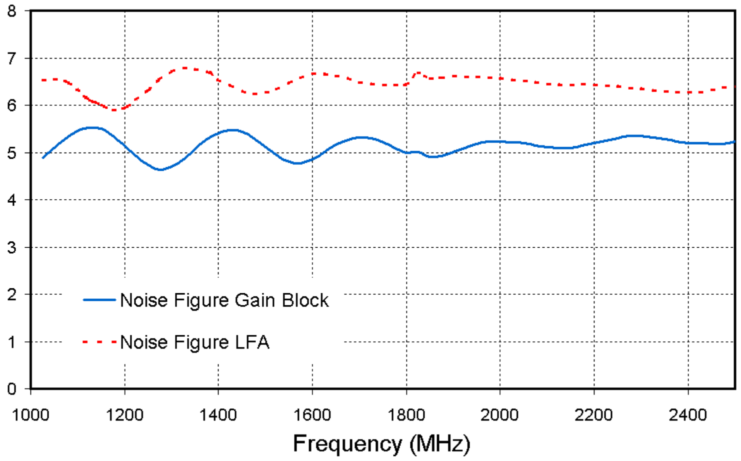


Figure 5.15 – Noise Figure of Gain-Block and Amplifier

The IIP3 of the amplifier is shown in Figure 5.16 with the improvement in IIP3 compared to the gain-block shown in Figure 5.17. The measured IIP3 of the amplifier can be seen to be greater than +14dBm from 1.4GHz to 2.5GHz and this is much worse than the simulated results that predict 21dB at 1.8GHz.

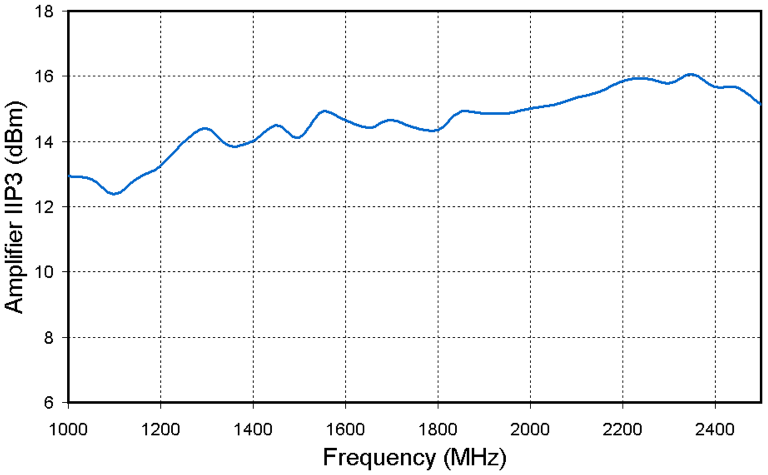


Figure 5.16 – Measured IIP3 of the Amplifier

The increase in IIP3 of the amplifier compared to the gain-block is 10dB over the design range of 1.5GHz to 2GHz. This is an excellent result and shows for the first time that this amplifier topology works and produces an improvement in IIP3 as expected with only a modest increase in the amplifier NF.

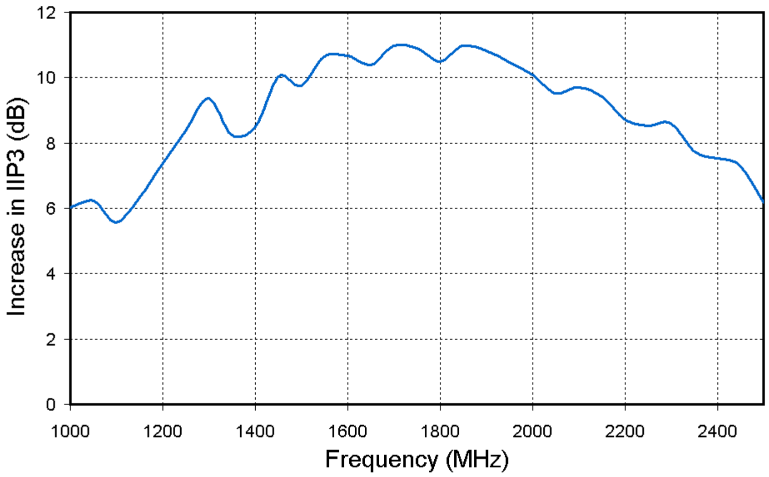


Figure 5.17 – Measured Increase in IIP3 of the Amplifier Compared to the Gain-Block

6 CONCLUSIONS AND CIRCUIT REDESIGN

6.1 Conclusions from Measured Results

Now that the circuits have been built, tested and compared to the simulated results, a number of conclusions can be drawn.

- The main aim of this Thesis was to describe the construction of an amplifier topology, referred to as a lossless-feedback or Norton-type of amplifier that has not previously been built on an IC. A procedure to design such an amplifier was presented and a suitable topology shown to work. The amplifier requires the design of two separate parts, a gain-block and an RF directional coupler. The gain and phase of both these parts needs to be carefully controlled for the amplifier to work.

  The tested amplifier works as expected with a flattening of the gain and an increase in the amplifier IIP3 as shown in Figure 6.1. It has not been possible to show if the simulated and measured results are in agreement because of the IC fabrication error, however the difference in performance of the amplifier compared to the gain-block was measured and presented. The feedback increases the IIP3 by over 10dB with a worsening in the NF by 1.2dB, which is entirely attributed to the extra losses associated with the directional coupler.

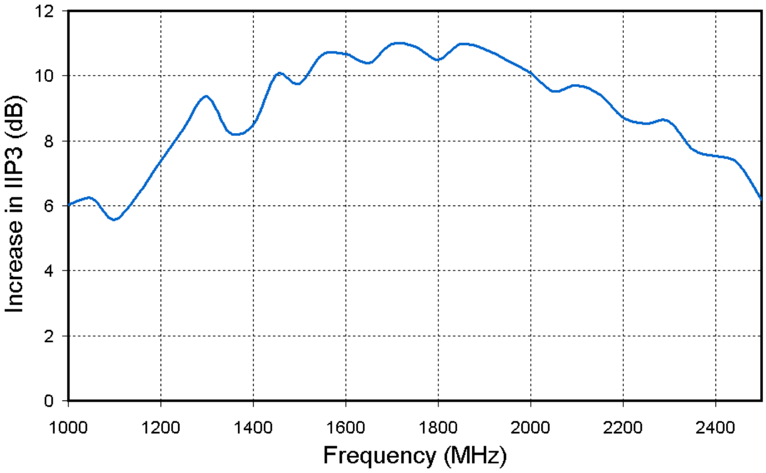


Figure 6.1 – Increase in IIP3 of the Norton Amplifier Compared to the Gain-Block without feedback.

- The fabricated IC was delivered with some major deviations from the nominal values that have severely affected the testing. The dominant error is the transistor gm that is approximately half that specified. Nevertheless testing proceeded by re-biasing the transistors at a higher supply voltage and drain currents, although the simulated and measured values can no longer be compared. UMC has admitted the fault as an N+ fabrication error [26] and are remaking the batch.
- The Discrete Component Coupler was shown to have good performance with excellent agreement between simulated and measured results. This is the first time, to the author's knowledge that such a circuit has been built and a paper describing its construction and performance has been submitted for publication [25]. This Thesis describes the design procedure for this coupler and this is repeated in Section 6.2.2.
- The Capacitors to ground were specifically designed with a large number of via connections going directly from M4 to M1 to have a good ground connection. This has resulted in a neater and smaller construction of the various circuit blocks. Measurements indicate that this component *may* have a Q up to 15-times better than the standard part.

- The inductive components were originally modeled incorrectly using a 6.2µm oxide thickness from the bottom of the M4-metal layer to the substrate. This dimension is not correct and should be 4.4µm as the metal layers under the transformers were blocked from forming. This allows better comparison to be made between the measured and simulated results although the differences are small.
- The Momentum simulator was found to give poor results when used to simulate parallel plate capacitors. This was shown during the simulation of standard UMC capacitor in section 3.3.1, where Momentum not only inaccurately calculates the capacitance value but also produces a solution that changes with the mesh size. In addition, the poor performance of the Transformer Coupler can be attributed to inaccurate Momentum simulations, where the simple capacitance equation was found to be more accurate than Momentum in calculating the interwinding capacitance.

6.2 Amplifier Redesign

The next step in this Thesis is to redesign the amplifier using the lessons learned from Chapter 5, and at the same time fix a number of deficiencies that were known with the original layout when submitted for fabrication. These deficiencies are listed below.

- The amplifier had no biasing circuits with two biasing voltages having to be generated externally. This is a reasonable approach while evaluating the topology but should be changed in a re-design. Two bias circuits are required, first a 0.7V gate voltage is required for TR1 and second, a current source needs to be provided to set the current through TR2.
- The gain of the amplifier design is low at between 7.1dB and 8.2dB and should be increased to a nominal 10dB to make the amplifier useful.
- The supply voltage was designed for 1.25V and was set at this low level in the original design to give some flexibility during testing and to give reasonable power consumption results. This voltage should now be increased to a more commonly used supply voltage, with the suggestion that 2.5V is a reasonable goal as this is the specification for IC fabrication process
- The inductor that dominates the layout of the gain-block and amplifier should be replaced with a smaller part to reduce the fabrication cost.

6.2.1 General

The redesigned amplifier is shown in Figure 6.2. The gain circuit now uses three transistors, with T1 and T3 connected in a cascode configuration to provide higher gain, and these are followed by T2 in a source follower configuration to lower the output impedance to be closer to 50-Ohm as well providing some reverse isolation to the tuned circuit components. This circuit configuration is similar to the original tested amplifier but with the addition of the cascode transistor to increase the amplifier gain.

The cascode circuit introduces some unwanted phase rotation in the forward path gain of the gain-block circuit that needs to be considered in the design, and this is the contributing reason for reduction in stability as shown by µ and µ’ in Figure 6.5. However the phase change is acceptable, as the phase rotation through the second FET T3 is small.

The amplifier is also designed to run at 2.5V, with it now taking 6.8mA in the cascode stage and 8mA in the source-follower. Two bias circuits are now included in the design. A P-Channel FET T4 sets the gate-voltage on T1 to achieve a constant bias current. This control circuit sets the voltage at point ‘**A**’ on the schematic to a constant value. The reference voltage for this circuit is the gate voltage of T4 that is set to half the supply voltage using two identical resistors.

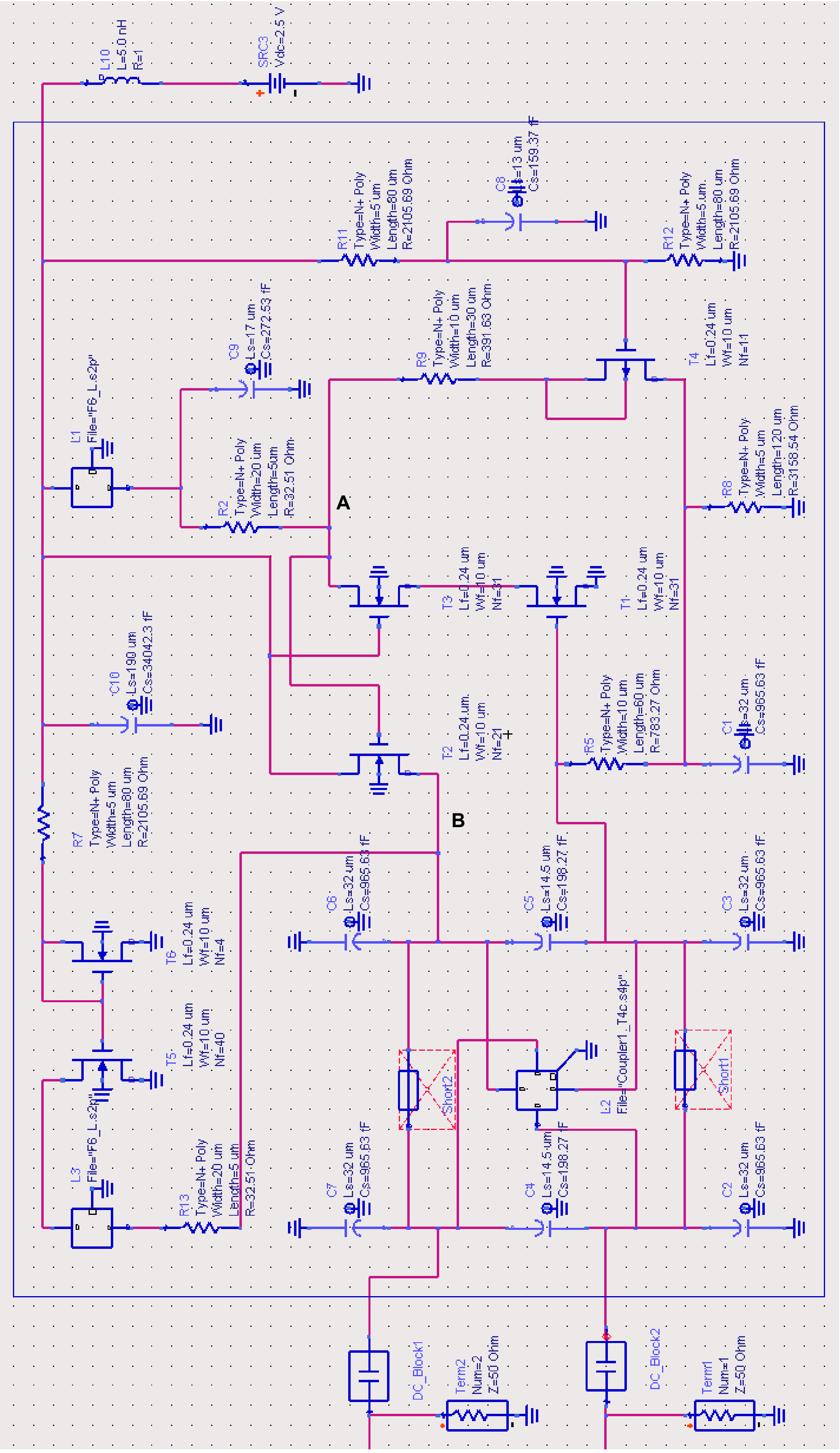

L10
L=5.0 nH
R=1
SRC3
Vdc=2.5 V
R11
Type=N+ Poly
Width=5 um
Length=80 um
R=2105.69 Ohm
C8
Ls=13 um
Cs=159.37 fF
R12
Type=N+ Poly
Width=5 um
Length=80 um
R=2105.69 Ohm
L1
File="F6_L.s2p"
C9
Ls=17 um
Cs=272.53 fF
R9
Type=N+ Poly
Width=10 um
Length=30 um
R=391.63 Ohm
T4
Lf=0.24 um
Wf=10 um
Nf=11
R2
Type=N+ Poly
Width=20 um
Length=5um
R=32.51 Ohm
A
R8
Type=N+ Poly
Width=5 um
Length=120 um
R=3158.54 Ohm
T3
Lf=0.24 um
Wf=10 um
Nf=31
T1
Lf=0.24 um
Wf=10 um
Nf=31
C10
Ls=190 um
Cs=34042.3 fF
T2
Lf=0.24 um
Wf=10 um
Nf=21
R5
Type=N+ Poly
Width=10 um
Length=60 um
R=783.27 Ohm
C1
Ls=32 um
Cs=965.63 fF
R7
Type=N+ Poly
Width=5 um
Length=80 um
R=2105.69 Ohm
B
C6
Ls=32 um
Cs=965.63 fF
C5
Ls=14.5 um
Cs=198.27 fF
C3
Ls=32 um
Cs=965.63 fF
T6
Lf=0.24 um
Wf=10 um
Nf=4
T5
Lf=0.24 um
Wf=10 um
Nf=40
Short2
L2
File="Coupler1_T4c.s4p"
Short1
L3
File="F6_L.s2p"
R13
Type=N+ Poly
Width=20 um
Length=5 um
R=32.51 Ohm
C7
Ls=32 um
Cs=965.63 fF
C4
Ls=14.5 um
Cs=198.27 fF
C2
Ls=32 um
Cs=965.63 fF
DC_Block1
Term2
Num=2
Z=50 Ohm
DC_Block2
Term1
Num=1
Z=50 Ohm

Figure 6.2 – Schematic of Updated Amplifier using a Cascode Configuration for the Gain Block and with the bias circuits included on the IC

In addition a current source has been added to bias the source follower transistor T2 and this is built using a simple current mirror with transistors T6 and T5. The reference current into T6 set to 800uA by the series resistor R7. The ratio of the transistor sizes sets the required output current.

The biasing is connected to point '**B**' on the IC because the RF impedance at this point is lower and hence the biasing components will have less influence on the circuit performance. The output impedance of the gain-block is 19.8-Ohm; whereas the output impedance from Figure 6.6 of the full amplifier is 49.7-Ohm. Connecting the current source to the 19.8-Ohm point is a better design solution.

6.2.2 RF Directional Coupler

The input RF directional coupler is unchanged from the original design, with the exception that the simulations are now carried out using a 4.4µm dimension from the bottom of the M4 metal layer to the substrate, and with nominal resistivity values. The design of the coupler was made using a number of well-defined steps and it is worth reiterating these steps here.

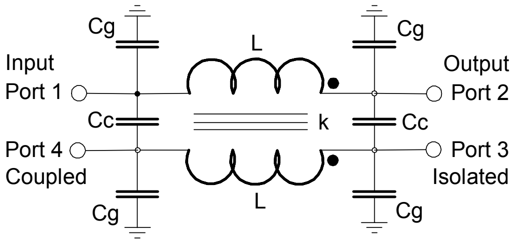


Figure 6.3 – Discrete Component Coupler

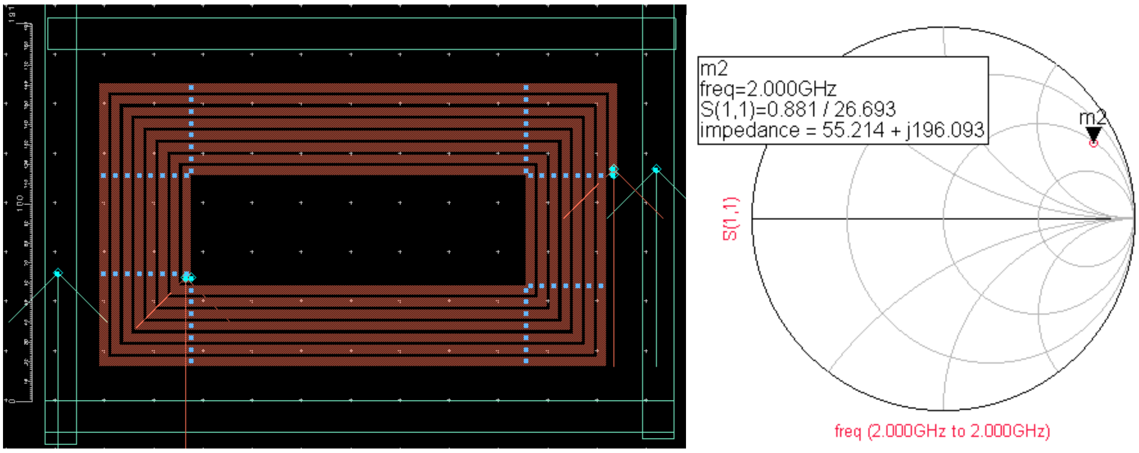
1. The center frequency of the RF directional coupler needs to be set above the required operating point of the amplifier to compensate for the phase rotation in the RF amplifier. In this example it was set 40% above the required operating frequency of 1.8GHz resulting in a 2.5GHz coupler.
2. The equations to calculate the circuit values can be found from the MathCAD sheet on page 88. This sheet calculates gives the inductance, capacitance and the mutual coupling for a required coupling level.
3. The inductor size can be initially estimated by using the MathCAD sheet on page 91 for a square inductor or from the following web page available from Stanford university that has a choice of inductor shapes: http://smirc.stanford.edu/spiralcalc.html. After the initial estimate is made, a Momentum simulation needs to be made to optimize the inductor to required value and to include the tracking to the inductor. Various track widths may be tried to minimize the series resistance as this will affect the path losses in the finished coupler.
4. Once the shape of the inductor is established, this shape is then copied to a second layer and further simulations run each generating a 4-port s-parameter file.
5. The transformer overlapping areas need to be measured and the capacitance associated with these calculated according to the simple capacitance equation. This is then subtracted from Cc.
6. In a similar way the capacitance to ground estimated and subtracted from Cg.
7. A second simulation circuit needs to be built where these capacitors are added and where the four-port S-parameter file can be imported. This circuit should also include an ideal transformer where the coupling coefficient is set, to allow a comparison of both circuit performances.

8. The coupling inductors from (4) above are adjusted in their overlap, a momentum simulation is run and the results compared to the ideal circuit. This is repeated until the two simulations are identical. At this point the transformer design is complete.

6.2.3 Design of Inductor

The spiral inductor that dominates the layout in the original circuit could be replaced with a specifically designed inductor that occupies less area. The starting point for this is knowing the current taken by the cascode amplifier circuit, T1 & T3, as this affects the track width that can be used in the design of the inductor.

The current at 6.8mA should not exceed a current density on the M5 layer of 1.5mA/µm [ref 27 page 23] and this defines a minimum track width of 4.5µm. With the track width chosen, the inductor is designed to have 7-turns, a spacing of 1.5µm and this can be seen in Figure 6.3. The outside dimensions of the inductor to the guard ring are 150µm by 350µm. The inductor performance can be seen in Figure 6.4 for one end shorted to ground and is equivalent to a 55-Ohm plus 7.6nH, which corresponds to an impedance of greater than 200-Ohm at 2GHz.



m2
freq=2.000GHz
S(1,1)=0.881 / 26.693
impedance = 55.214 + j196.093

Figure 6.4– Impedance of Inductor L1 showing the equivalent circuit of a 55-Ohm series resistor in series with a 7.6nH inductor.

6.2.4 Performance Simulations

The circuit performance of the amplifier can be seen in Figures 6.5. The NF of the amplifier is 2.7dB at 1.8GHz; which is the NF of the gain-block at 1.59dB plus the losses in the RF directional coupler at 1.2dB. The stability of the gain-block is unconditional, whereas the stability of the amplifier is not with certain source & load impedances that could result in oscillation. The gain of the final amplifier is 9.8dB compared to a peak gain of 23dB in the gain-block and the input and output impedances for the amplifier have a VSWR of less than 2:1

The final amplifier has an IIP3 of between +9 and +15dBm from 1.5 to 2GHz. In addition the increase in IIP3 can be seen in Figure 6.6 and this shows that an increase of over 16dB is obtained above 1.5GHz.

It is possible to operate this amplifier up 2.5GHz where the NF stays below 3dB. At 2.4GHz the amplifier has a NF of 3dB, a gain of 9dB and an IIP3 of +19dBm, these are excellent results, assuming I want a 2.4GHz amplifier.

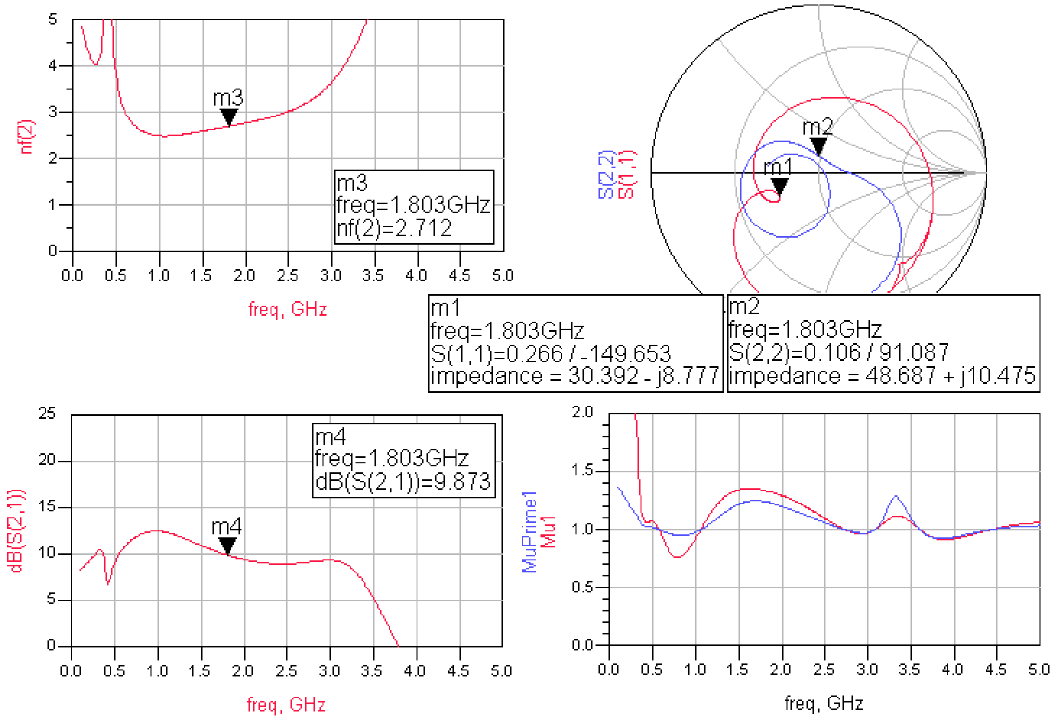


Figure 6.5 Simulated Performance of the Amplifier

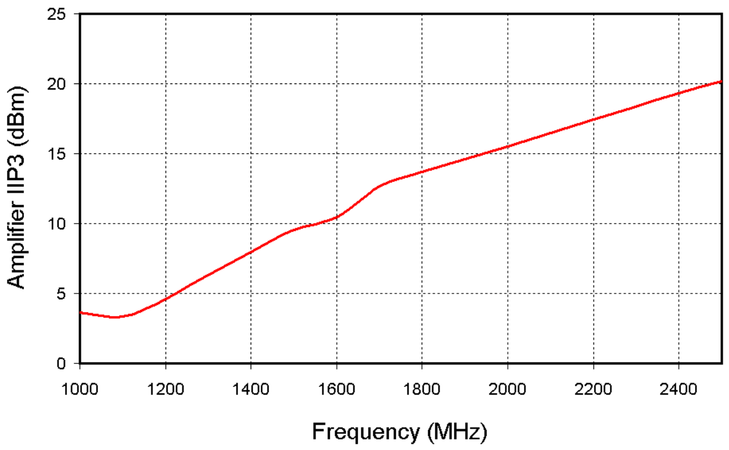


Figure 6.6 – IIP3 of the Redesigned Amplifier

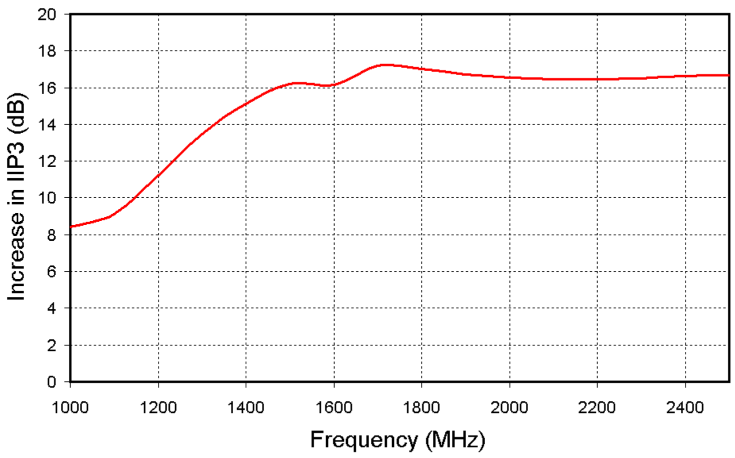


Figure 6.7 – Increase in IIP3 of the Redesigned Amplifier Compared to the IIP3 of the Gain-Block

6.3 Transformer Coupler Redesign

The final step in the Thesis is to consider a redesign of the Transform RF Directional Coupler to overcome the problem of interwinding capacitance that was found during testing. There are two ways that this can be done, either the two windings can be moved further apart, or the track width of the secondary winding can be reduced with more space between the turns.

In this design iteration both options are taken, the top tracking is left unchanged and the secondary winding is moved from the M4 to the M2 layer, which is 3µm below M5. In addition the track width of the secondary winding is reducing to 6µm with a spacing of 5µm between turns, the number of turns is left unchanged at 7. A Momentum simulation is constructed using the MRINDNBR shape for the secondary winding, with Ns=28, L=260µm, W=6µm and S=5µm. The construction can be seen in Figure 6.8.

The simulation results are saved as a 3-port S-parameter file and first checked for interwinding capacitance using the ADS circuit shown in Figure 5.12. The capacitance comes to 0.37pF, which is close to 0.413pF obtained from the MathCAD sheet on page 95 implying that the interwinding capacitance in the S-parameter file is reasonably correct and this should result in an accurate simulation.

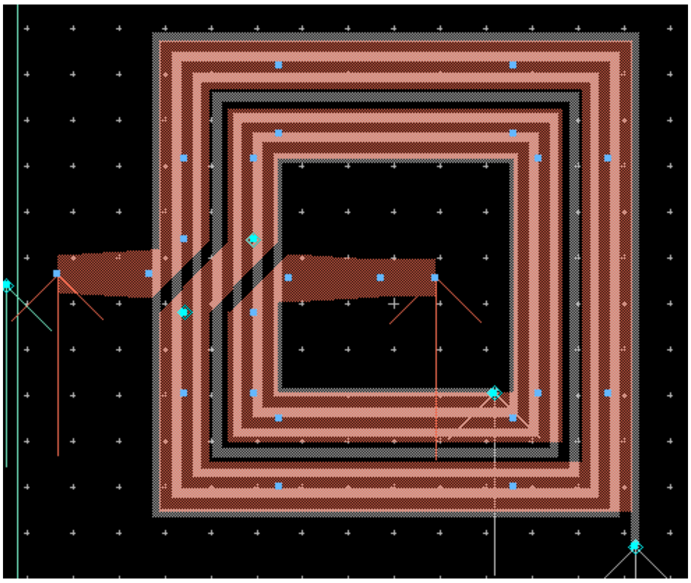


Figure 6.8 – Proposed Construction for the redesign of Transformer Coupler. The metal-5 layer is unchanged; the secondary winding is moved to metal-2 with reduced track width.

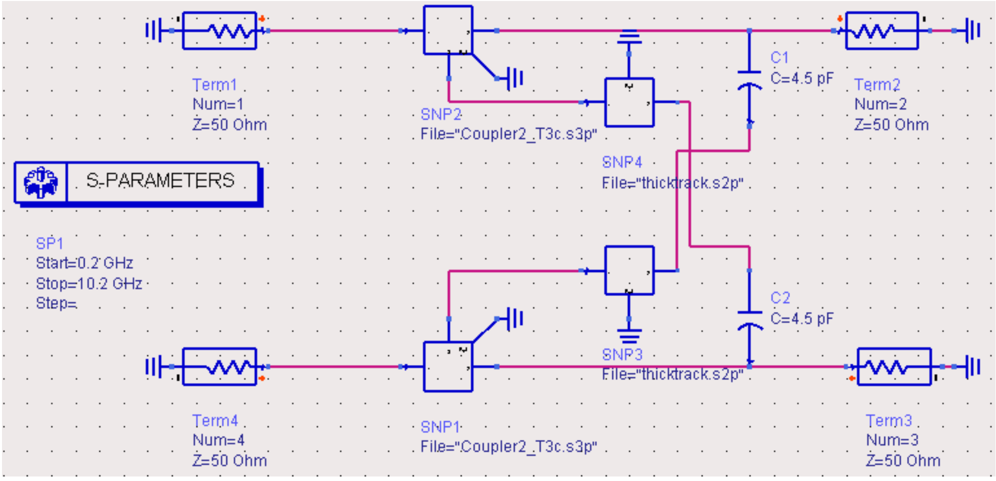

Term1
Num=1
Z=50 Ohm
SNP2
File="Coupler2_T3c.s3p"
C1
C=4.5 pF
Term2
Num=2
Z=50 Ohm
S-PARAMETERS
SNP4
File="thicktrack.s2p"
SP1
Start=0.2 GHz
Stop=10.2 GHz
Step=
C2
C=4.5 pF
SNP3
File="thicktrack.s2p"
Term4
Num=4
Z=50 Ohm
SNP1
File="Coupler2_T3c.s3p"
Term3
Num=3
Z=50 Ohm

Figure 6.9 – Simulation Circuit for New Transformer Coupler.

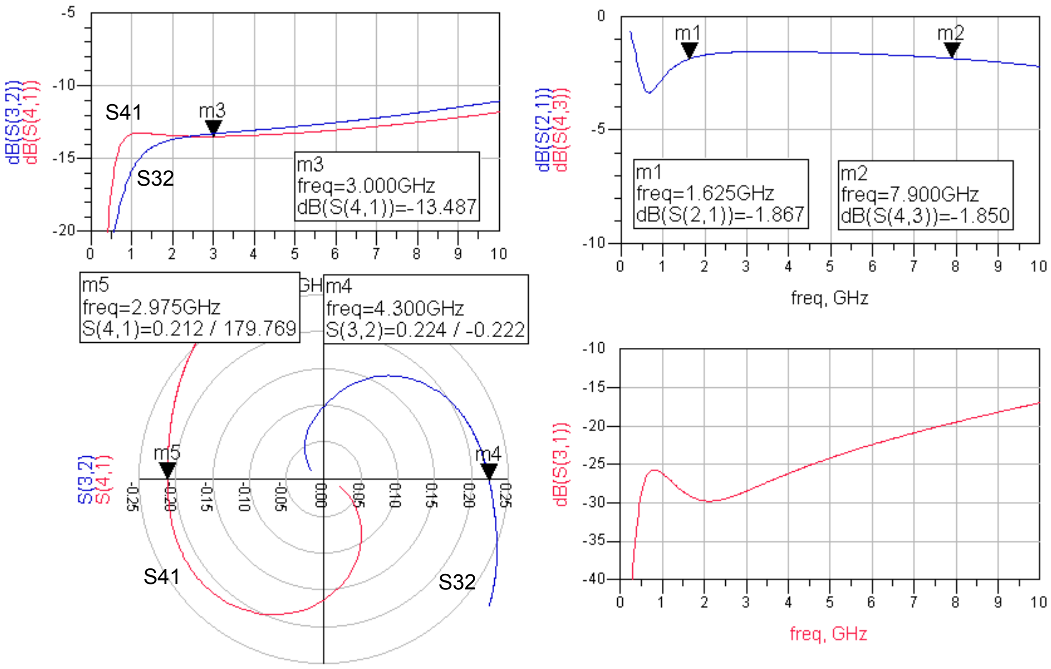


Figure 6.10 Simulation Results for New Transformer Coupler

The ADS simulation circuit is shown in Figure 6.9 and the results can be found in Figure 6.10. The results show that a wide bandwidth is obtained from 1.6GHz to 7.9GHz, with a forward path loss of 1.8dB with a variation of 0.3dB across this band. The coupling power, S32 is –13.5dB at 3GHz with 3dB variation across the band and with a good phase response, with 0-degrees of phase rotation at 4.3GHz. The alternative coupled port S41 is of inverted phase with 180-degrees of phase rotation at 3GHz. The amplitude response of S41 is also flatter and has a wider bandwidth. The reverse isolation, S31 is better than 20dB up to 7GHz.

The simulation results show that the response is acceptable down to 1.6GHz but below this a number of parameters diverge from the optimum. If the frequency response of the coupler is to be extended down in frequency, the size of the coupler will need to be increased.

Moving the secondary winding further away from the primary, and reducing the track thickness has reduced the interwinding capacitance, but has also reduced the coupling and this may go someway to explain why the S32 coupled power is –13.5dB, whereas the design equations from the MathCAD sheet on page 93 indicate that –11dB should be obtained. It is interesting to note that to increase the RF coupled power, the number of secondary turns should be *reduced* and not increased.

The Cadence design of the coupler has been updated to reflect these changes and this is shown in Figure 6.11. The secondary winding is moved to Metal-2 and reduced to 6µm; the track from the capacitor to the opposite RF connection is increased in width to 10µm. Other than these changes the design is unmodified.

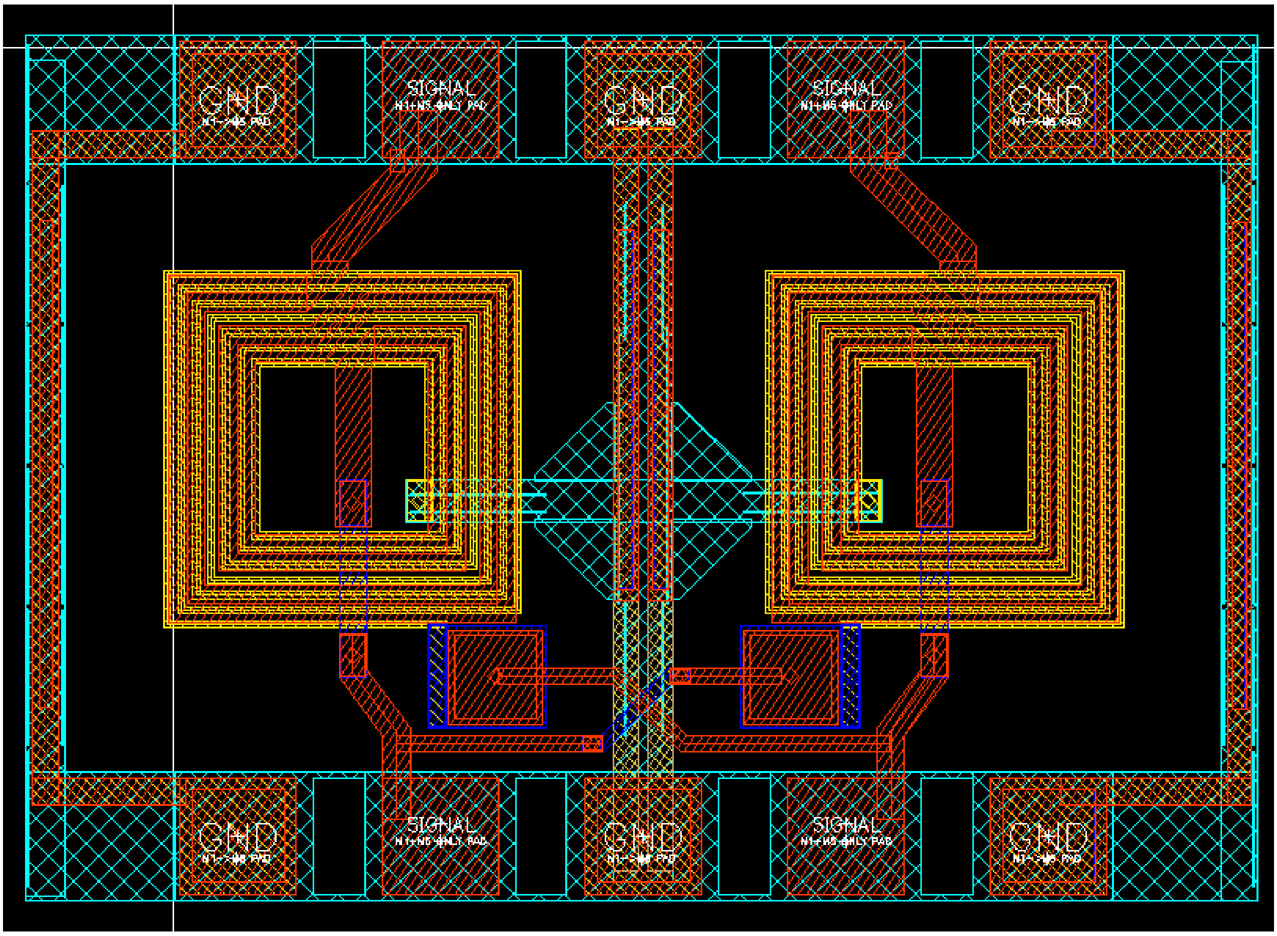

GND
N1->N5 PAD
SIGNAL
N1+N5 ONLY PAD
GND
N1->N5 PAD
SIGNAL
N1+N5 ONLY PAD
GND
N1->N5 PAD
GND
N1->N5 PAD
SIGNAL
N1+N5 ONLY PAD
GND
N1->N5 PAD
SIGNAL
N1+N5 ONLY PAD
GND
N1->N5 PAD

Figure 6.11 – Updated Transformer Coupler Layout

REFERENCES.

1 Norton D., “High Dynamic Range Amplifier”, US Patent 3624536, 1971, Anzac Corporation

2 R. Frye, S Kapur, R Melville, “A 2 GHz Quadrature Hybrid implemented in CMOS Technology”, IEEE JSSC, March 2003, P550.

3 David M Pozar, “Microwave and RF Design of Wireless Systems”, Wiley, Chapters 3.5, 3.7, 6.2 and 6.3.

4 ETSI TS 100 910 V8.16.0 (2003-08), section 5.3, 6.2, Document name ts_100910v081600p.pdf

5 Edward M & Sinsky J, “A new criterion for linear 2-port stability using geometrically derived parameters”, IEE MTT, Volume 40, p2303, Dec 1992..

6 Abrie P, “Design of RF Microwave Amplifiers & Oscillators”.

7 Mead H. B. & Callaway G. R., “Broadband Amplifier”, US Patent 4042887, 1977, Q-bit Corporation

8 Norton, D & Podell A, “Transistor Amplifier with Impedance-Matching Transformer”, US Patent 3891934, June 1975, Anzac Corporation

9 Long J & Copeland M, “A 1.9GHz Low-Voltage Silicon Bipolar Receiver Front-End for Personal Communications Systems”, IEEE Journal of Solid state Circuits, Volume 30, Dec 1995, P1438.

10 Nosal Z., “The Design of Low Noise GaAs MMIC Broadband Amplifiers”, IEE reference 00740825

11 Yang X, Wu T, McMacken J, “Design of LNA at 2.4GHz using 0.25um Technology”, IEEE reference 00942333

12 MathCAD is a mathematic authoring program by MathSoft

13 HPADS or ADS is a circuit simulation tool by HP and includes a method-of-moments tool called Momentum. The circuits analyzed in this Thesis are archived in LFA.ZAP, which is held in the ADS subdirectory. The list of simulation circuits is shown here.

14 Kajfez D, “Scattering matrix of a directional coupler with ideal transformers”, IEE Proc Microwaves & Antennas, volume 146, August 1999, page 295.

15 UMC, “UMC 0.25um 1P5M Salicide 2.5V RF Spice Models”, Table 3-5. Document name “UMC_25_2.5V_RF_Model_Document_v110.pdf”

16 UMC, “0.25um 2.5/3.3 1P5M RF CMOS Process Electrical Design Rule”, Document name “G-02-RFCMOS25-2.5V_3.3V-1P5M-EDR.PDF”

17 Hogerheiden J, Ciminera M, Jue G, “Improved Planar Spiral Transformer Theory Applied to Miniature Lumped Element Quadrature Hybrid”, IEEE MTT, Volume 45, April 1997, P453.

18 Goo, Ahn, et al, “A Noise Optimization Technique for Integrated Low Noise Amplifiers”, IEEE SSC, Volume 37, number 8, August 2002, page 994 onwards.

19 UMC, “0.25um 2.5/3.3V 1P5M RF CMOS Process Interconnect Capacitance Model”, Document name G-04-RFCMOS25-2.5V_3.3V-1P5M-INTERCAP.PDF

20 Thomas H. Lee, “The Design of Radio Frequency Integrated Circuits”, Cambridge University Press, chapter 2.3.

21 Okazaki H, Hirota T, “Multilayer MMIC Broad-Side Coupler with a Symmetric Structure”, IEEE, Microwave Guided Wave Letters, Vol 7, number 6, June 1997, p145.

22 Coupler design used in RF simulated RFSim.

23 70 Ohm N+Poly Resistor Design by Per Madsen a PhD student at Aalborg University on which the resistors designed in this thesis are based.

24 Cadence is the layout tool used in the design of these IC’s. The layer definitions are shown here.

25 C Haji-Michael, O Jensen, J Mikkelsen, ‘An RF Directional Coupler Using Lumped Elements’

26 Email from Jan Mikkelsen reporting fabrication fault found by UMC

27 UMC, “0.25um 2.5/3.3V 1P5M RF CMOS Process Topological Layout Rule FAB8E”, Document name G-03-RFCMOS25-2.5V_3.3V-1P5M-TLR-8E.PDF

28 Thomas Lee, “The VLSI Handbook, section 15.4, On-chip Transformers”, CRC Press, Editor Wai-Kai Chen.

29 Troels Emil Kolding, “On Wafer Measuring Techniques for Characterizing RF CMOS Devices”, PhD Thesis RISC group, Aalborg University 1999.

APPENDIX A MATHCAD SHEETS

MathCAD is a product from MathSoft that combines mathematics capabilities with the WYSIWYG interface of a word processor. The following MathCAD sheets were created for this project, an image of these sheets can be found in this Appendix and the files are available on an attached CD ROM. A viewer for these files has also been included but does not work with all files.

Page	Description	File Name
86	Values for Discrete Component Branchline Coupler (Type-1)	BranchLineCoupler-T1.mcd
87	Values for Discrete Component Branchline Coupler (Type-2)	BranchLineCoupler-T2.mcd
88	Values for Discrete Component Coupler	Discrete Comp Coup.mcd
89	Parallel Plate Capacitance Calculator	Parallel Plate Cap.mcd
91	Calculation for Planar Square Inductors	Planar Square Ind.mcd
93	Transformer Directional Coupler	Transformer Coupler.mcd
	Calculate Microstrip Line Impedance includes line thickness correction and dispersion	Zo.mcd
	Calculate Zoo & Zoe for coupled Microstrip	ZooZoe.mcd
95	Calculates Transformer coupler inter-winding capacitance according to the simple capacitance equation	Transformer Capacitance.mcd

Values for Discrete Component Branch Line Coupler (Type-1)

Chris Haji-Michael

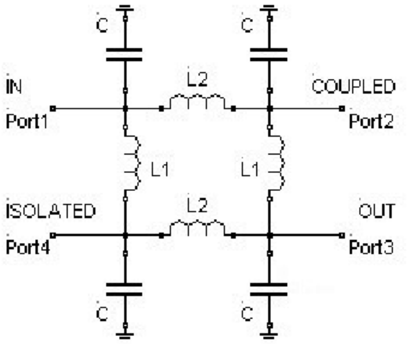
This page calculates the circuit values for a branch line coupler. The equations are from "Practical Microstrip Circuit Design", Trinogga, Kaizhou, Hunter, P363. In this coupler the wanted power goes from port 1 to port 3; coupled power goes to port 2.

$\mathrm{Freq} := 2.0\cdot 10^{9}\,\mathrm{Hz}$

$c := -2, -4 .. -16$ Coupling Ratio (power to port 2 wrt 3)

$\mathrm{Zo} := 50\mathrm{ohm}$

$\mathrm{nH} := 1\cdot 10^{-9}\,\mathrm{H}$



$k2(c) := 10^{\left(\frac{c}{10}\right)}$ $\qquad k3(c) := 1 - k2(c)$ $\qquad k(c) := \dfrac{k2(c)}{k3(c)}$

$Z1(c) := \mathrm{Zo}\cdot k(c)^{0.5}$ $\qquad Z2(c) := \left[\dfrac{(k(c))}{k(c)+1}\right]^{0.5}\mathrm{Zo}$

$\mathrm{LosstoP3}(c) := 10\cdot\log(k3(c))$

$L1(c) := Z1(c)\dfrac{1}{2\cdot\pi\cdot\mathrm{Freq}}$

$L2(c) := Z2(c)\dfrac{1}{2\cdot\pi\cdot\mathrm{Freq}}$

$CL1(c) := \dfrac{1}{Z1(c)}\cdot\dfrac{1}{2\cdot\pi\cdot\mathrm{Freq}}$

$CL2(c) := \dfrac{1}{Z2(c)}\cdot\dfrac{1}{2\cdot\pi\cdot\mathrm{Freq}}$

$C(c) := CL1(c) + CL2(c)$

c =	Z1(c) = ohm	Z2(c) = ohm
-2	65.38	39.72
-4	40.66	31.55
-6	28.96	25.06
-8	21.70	19.91
-10	16.67	15.81
-12	12.98	12.56
-14	10.18	9.98
-16	8.03	7.92

Z1 = port 1 to 4 (shunt)
Z2 = port 2 to 3 (series)

c =	L1(c) = nH	L2(c) = nH	C(c) = pF	LosstoP3(c) =
-2	5.20	3.16	3.22	-4.329
-4	3.24	2.51	4.48	-2.205
-6	2.30	1.99	5.92	-1.256
-8	1.73	1.58	7.67	-0.749
-10	1.33	1.26	9.81	-0.458
-12	1.03	1.00	12.47	-0.283
-14	0.81	0.79	15.79	-0.176
-16	0.64	0.63	19.96	-0.110

Values for Discrete Component Branch Line Coupler (Type-2)

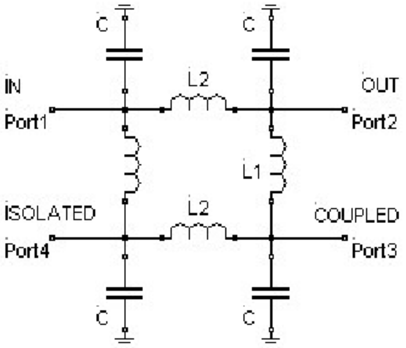
Chris Haji-Michael

This page calculates the circuit values for a branch line coupler. The equations are adapted from "Microwave Engineering using Microstrip", Fooks, Zakarevicius, P158. In this coupler the wanted power goes from port 1 to port 2; coupled to port 3.

$\mathrm{Freq} := 2.0 \cdot 10^{9}\,\mathrm{Hz}$

$c := -2, -4 .. -16$ Coupling Ratio (power to port 3 wrt 2)

$\mathrm{Zo} := 50\,\mathrm{ohm}$



$\mathrm{nH} := 1 \cdot 10^{-9}\,\mathrm{H}$

$\mathrm{k2}(c) := 10^{\left(\frac{c}{10}\right)}$ $\qquad \mathrm{k3}(c) := 1 - \mathrm{k2}(c)$ $\qquad k(c) := \frac{\mathrm{k2}(c)}{\mathrm{k3}(c)}$

$\mathrm{Z1}(c) := \left(\frac{1}{k(c)^{0.5}}\right) \cdot \mathrm{Zo}$ $\qquad \mathrm{Z2}(c) := \left(\frac{1}{k(c)+1}\right)^{0.5} \mathrm{Zo}$

$\mathrm{LosstoP2}(c) := 10 \cdot \log(\mathrm{k3}(c))$

$\mathrm{L1}(c) := \mathrm{Z1}(c) \frac{1}{2 \cdot \pi \cdot \mathrm{Freq}}$

$\mathrm{L2}(c) := \mathrm{Z2}(c) \frac{1}{2 \cdot \pi \cdot \mathrm{Freq}}$

$\mathrm{CL1}(c) := \frac{1}{\mathrm{Z1}(c)} \cdot \frac{1}{2 \cdot \pi \cdot \mathrm{Freq}}$

$\mathrm{CL2}(c) := \frac{1}{\mathrm{Z2}(c)} \cdot \frac{1}{2 \cdot \pi \cdot \mathrm{Freq}}$

$C(c) := \mathrm{CL1}(c) + \mathrm{CL2}(c)$

c =	Z1(c) =		Z2(c) =	
-2	38.24	ohm	30.37	ohm
-4	61.48		38.79	
-6	86.33		43.27	
-8	115.21		45.87	
-10	150.00		47.43	
-12	192.67		48.4	
-14	245.55		48.99	
-16	311.49		49.37	

Z1 = port 1 to 4 (shunt)
Z2 = port 2 to 3 (series)

c =	L1(c) =		L2(c) =		C(c) =		LosstoP2(c) =
-2	3.04	nH	2.42	nH	4.70	pF	-4.329
-4	4.89		3.09		3.35		-2.205
-6	6.87		3.44		2.76		-1.256
-8	9.17		3.65		2.43		-0.749
-10	11.94		3.77		2.21		-0.458
-12	15.33		3.85		2.06		-0.283
-14	19.54		3.90		1.95		-0.176
-16	24.79		3.93		1.87		-0.110

Values for Discrete Component Coupler

Chris Haji-Michael

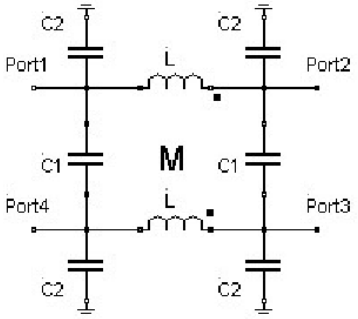
This page calculates the component vales for a 90 degree discrete component directional coupler. The circuit is shown below. The equations are from "Improved Planar Spiral Transformer Theory..." IEEE MTT, April 1997, p543 and from hand notes from Ole Kiel Jensen at Aalborg University.

$\mathrm{Freq} := 2.5\cdot 10^{9}\,\mathrm{Hz}$

$c := -10, -11 .. -16$ Coupling in dB from port 2 to 3.

$\mathrm{Zo} := 50\mathrm{ohm}$

$\mathrm{nH} := 1\cdot 10^{-9}\,\mathrm{H}$



$$\mathrm{Zoe}(c) := \mathrm{Zo}\cdot\left[\frac{\left(1+10^{\frac{c}{20}}\right)}{\left(1-10^{\frac{c}{20}}\right)}\right]^{0.5} \qquad \mathrm{Zoo}(c) := \mathrm{Zo}\cdot\left[\frac{\left(1-10^{\frac{c}{20}}\right)}{\left(1+10^{\frac{c}{20}}\right)}\right]^{0.5}$$

$$\mathrm{C1}(c) := \left(\frac{1}{\mathrm{Zoo}(c)}-\frac{1}{\mathrm{Zoe}(c)}\right)\frac{1}{4\cdot\pi\cdot\mathrm{Freq}} \qquad \mathrm{C2}(c) := \frac{1}{\mathrm{Zoe}(c)}\cdot\frac{1}{2\cdot\pi\cdot\mathrm{Freq}} \qquad \mathrm{L}(c) := (\mathrm{Zoo}(c)+\mathrm{Zoe}(c))\frac{1}{4\cdot\pi\cdot\mathrm{Freq}}$$

$$\mathrm{M}(c) := \frac{(\mathrm{Zoe}(c)-\mathrm{Zoo}(c))\cdot 1}{2\cdot\pi\cdot\mathrm{Freq}}$$ Mutual Inductance

$$\mathrm{k}(c) := \frac{\mathrm{Zoe}(c)-\mathrm{Zoo}(c)}{\mathrm{Zoe}(c)+\mathrm{Zoo}(c)}$$ Inductor Coupling

c =	Zoo(c) =		Zoe(c) =	
-10	36.038	ohm	69.371	ohm
-11	37.425		66.800	
-12	38.681		64.632	
-13	39.817		62.787	
-14	40.845		61.207	
-15	41.774		59.845	
-16	42.614		58.666	

c =	C1(c) =		C2(c) =		L(c) =		k(c) =	M(c) =	
-10	0.424	pF	0.918	pF	3.355	nH	0.316	2.12	nH
-11	0.374		0.953		3.318		0.282	1.87	
-12	0.330		0.985		3.289		0.251	1.65	
-13	0.292		1.014		3.266		0.224	1.46	
-14	0.259		1.040		3.248		0.200	1.30	
-15	0.230		1.064		3.235		0.178	1.15	
-16	0.204		1.085		3.224		0.158	1.02	

Parallel Plate Capacitance Calculator

Chris Haji-Michael

This sheet is used to calculate the capacitance obtained from parallel plate capacitors. The values for metal Thickness and Depth are from the UMC CMOS IC fabracation process used by Aalborg University. These formulas are from the VLSI handbook.

The depth (d) is taken from this document from UMC
G-02-RFCMOS25-2.5V_3.3V-1P5M-EDR.PDF
Which gives the depth (MMC to M4) as 450 to 550A

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$\mathrm{um} := 10^{-6}\,\mathrm{m}$

$\mathrm{Depth} := 0.050\cdot\mathrm{um}$

$\mathrm{Width} := 1\cdot\mathrm{um}, 2\cdot\mathrm{um} .. 100\cdot\mathrm{um}$

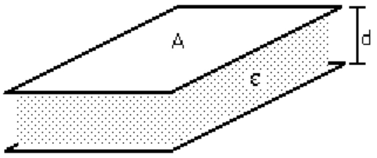
$\varepsilon_r := 4.1$

$\mathrm{Thickness} := 0.15\mathrm{um}$

$\varepsilon_o := 8.854187817\cdot 10^{-12}\cdot\dfrac{\mathrm{farad}}{\mathrm{m}}$

$\mathrm{fF} := 10^{-15}\,\mathrm{F}$

$\mathrm{Length} := \mathrm{Width}$



Conventional

$$\mathrm{ConventionalC}(\mathrm{Width},\mathrm{Length}) := \frac{\varepsilon_r\cdot\varepsilon_o\cdot\mathrm{Width}\cdot\mathrm{Length}}{\mathrm{Depth}}$$

Yuan's Formula

$$\mathrm{YuanC}(\mathrm{Width},\mathrm{Length}) := \varepsilon_r\cdot\varepsilon_o\left[\frac{\mathrm{Width}}{\mathrm{Depth}} + \frac{2\cdot\pi}{\ln\left[1+\left(\frac{2\cdot\mathrm{Depth}}{\mathrm{Thickness}}\right)\cdot\left(1+\sqrt{1+\frac{\mathrm{Thickness}}{\mathrm{Depth}}}\right)\right]} - \frac{\mathrm{Thickness}}{2\cdot\mathrm{Depth}}\right]\cdot\mathrm{Length}$$

Sakurai's Formula

$$\mathrm{SakuraiC}(\mathrm{Width},\mathrm{Length}) := \varepsilon_r\cdot\varepsilon_o\cdot\left[\frac{\mathrm{Width}}{\mathrm{Depth}} + 0.15\cdot\frac{\mathrm{Width}}{\mathrm{Depth}} + 2.8\cdot\left(\frac{\mathrm{Thickness}}{\mathrm{Depth}}\right)^{0.222}\right]\cdot\mathrm{Length}$$

Meijs & Fokkema Formula

$$\mathrm{MFC}(\mathrm{Width},\mathrm{Length}) := \varepsilon_r\cdot\varepsilon_o\cdot\left[\frac{\mathrm{Width}}{\mathrm{Depth}} + 0.77 + 1.06\cdot\left[\left(\frac{\mathrm{Width}}{\mathrm{Depth}}\right)^{0.25} + \left(\frac{\mathrm{Thickness}}{\mathrm{Depth}}\right)^{0.5}\right]\right]\cdot\mathrm{Length}$$

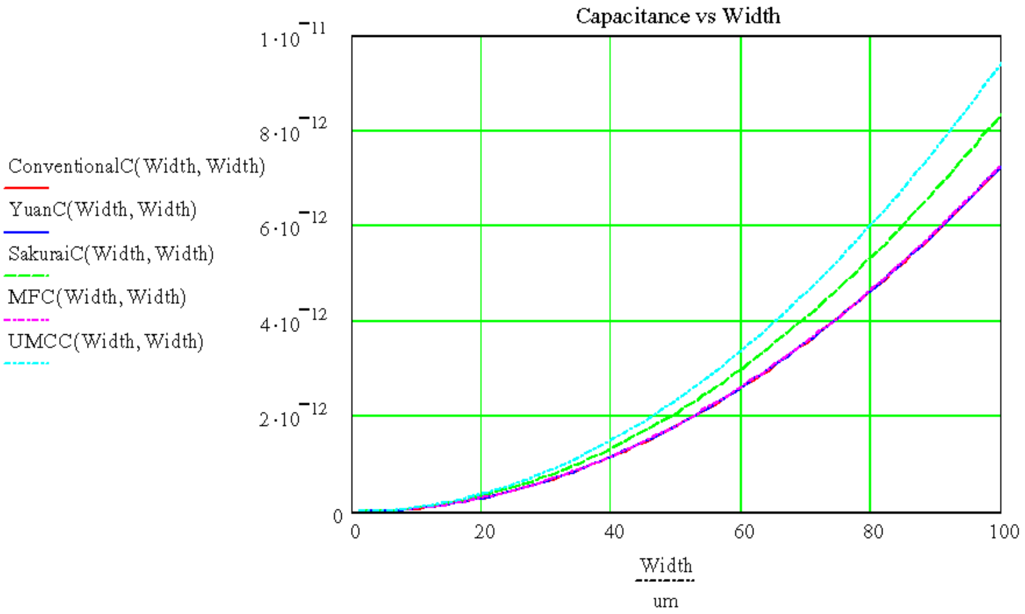
UMC Scaling Formula

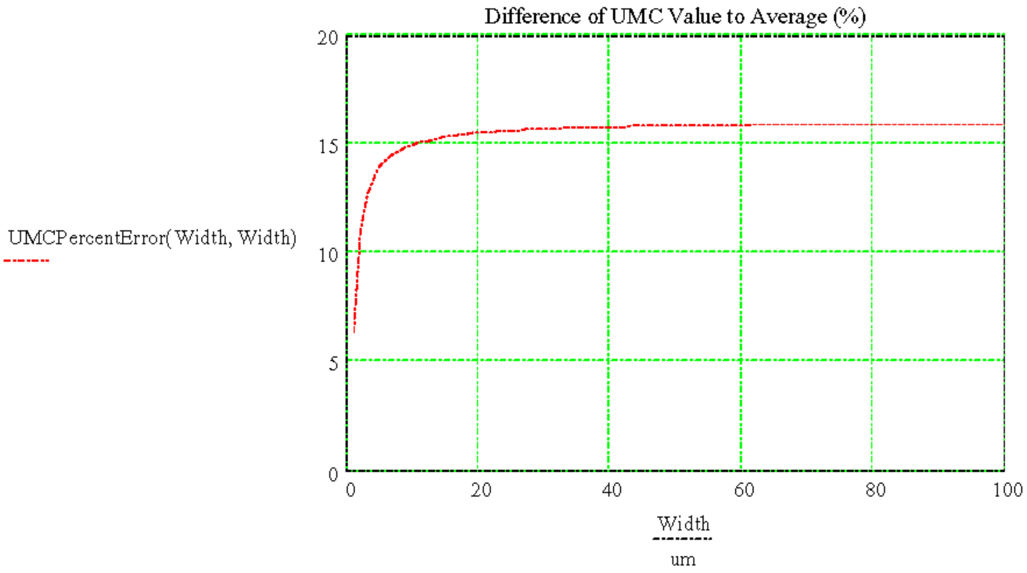
$$\mathrm{UMCC}(\mathrm{Width},\mathrm{Length}) := 0.943\cdot\mathrm{Width}\cdot\mathrm{Length}\cdot 10^{-3}$$

Average Capacitance & Calculation of Error

$$\mathrm{AverageC}(\mathrm{Width},\mathrm{Length}) := \frac{1}{5}\left(\begin{array}{l}\mathrm{ConventionalC}(\mathrm{Width},\mathrm{Length}) + \mathrm{YuanC}(\mathrm{Width},\mathrm{Length}) \ldots \\ + \mathrm{SakuraiC}(\mathrm{Width},\mathrm{Length}) + \mathrm{MFC}(\mathrm{Width},\mathrm{Length}) + \mathrm{UMCC}(\mathrm{Width},\mathrm{Length})\end{array}\right)$$

$$\mathrm{UMCPercentError}(\mathrm{Width},\mathrm{Length}) := \left(\frac{\mathrm{UMCC}(\mathrm{Width},\mathrm{Length}) - \mathrm{AverageC}(\mathrm{Width},\mathrm{Length})}{\mathrm{UMCC}(\mathrm{Width},\mathrm{Length})}\right)\cdot 100$$


Capacitance vs Width
ConventionalC(Width, Width)
YuanC(Width, Width)
SakuraiC(Width, Width)
MFC(Width, Width)
UMCC(Width, Width)
1·10⁻¹¹
8·10⁻¹²
6·10⁻¹²
4·10⁻¹²
2·10⁻¹²
0
0
20
40
60
80
100
Width
um


Difference of UMC Value to Average (%)
UMCPercentError(Width, Width)
20
15
10
5
0
0
20
40
60
80
100
Width
um

Calculation for Planar Square Inductors

Chris Haji-Michael

This page is to assist in the design of planar spiral inductors type d. The expressions are from this paper in the IEEE Journal of Solid State Circuits, October 1999.

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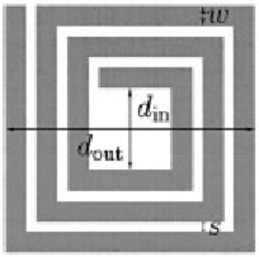
$\mu m := 1 \cdot 10^{-6} m \qquad nH := 1 \cdot 10^{-9} \cdot H \qquad \mu_0 := 4 \cdot \pi \cdot 10^{-7} \cdot newton \cdot amp^{-2}$

$d_{in} := 40 \cdot \mu m, 55 \cdot \mu m .. 300 \cdot \mu m$



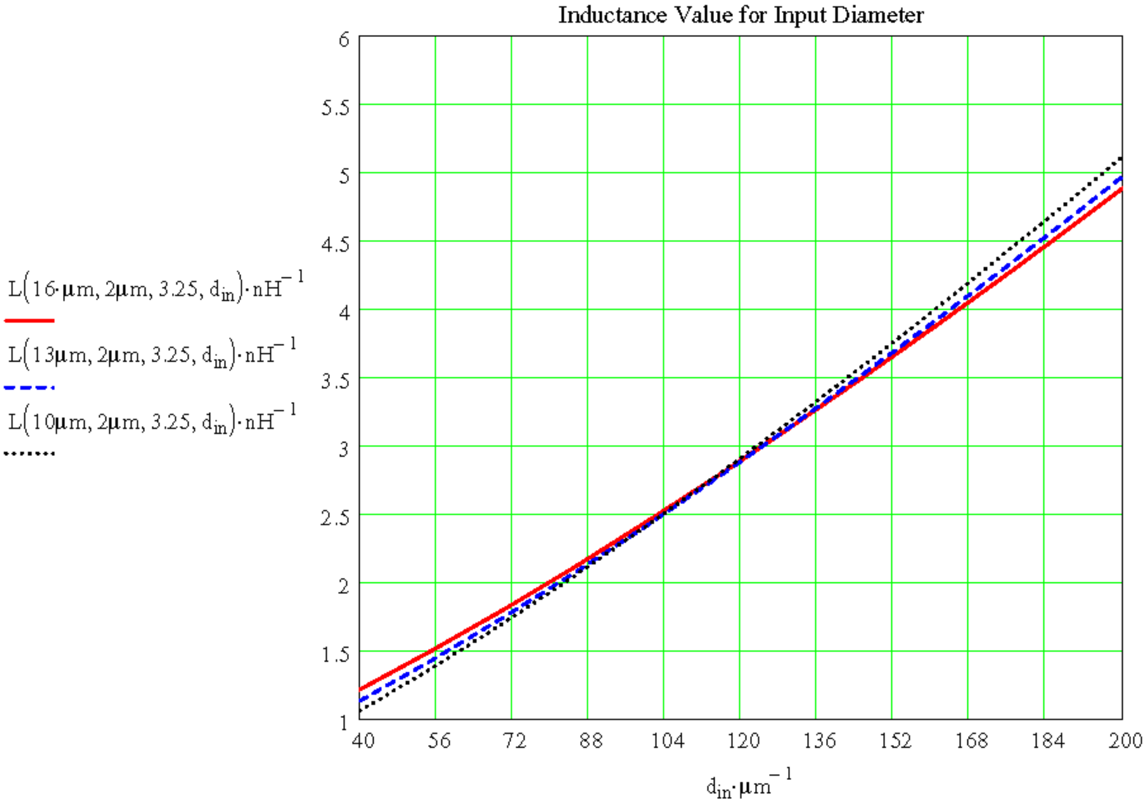
(a)

$C_{a1} := 1.27 \quad C_{a2} := 2.07 \quad C_{a3} := 0.18 \quad C_{a4} := 0.13$

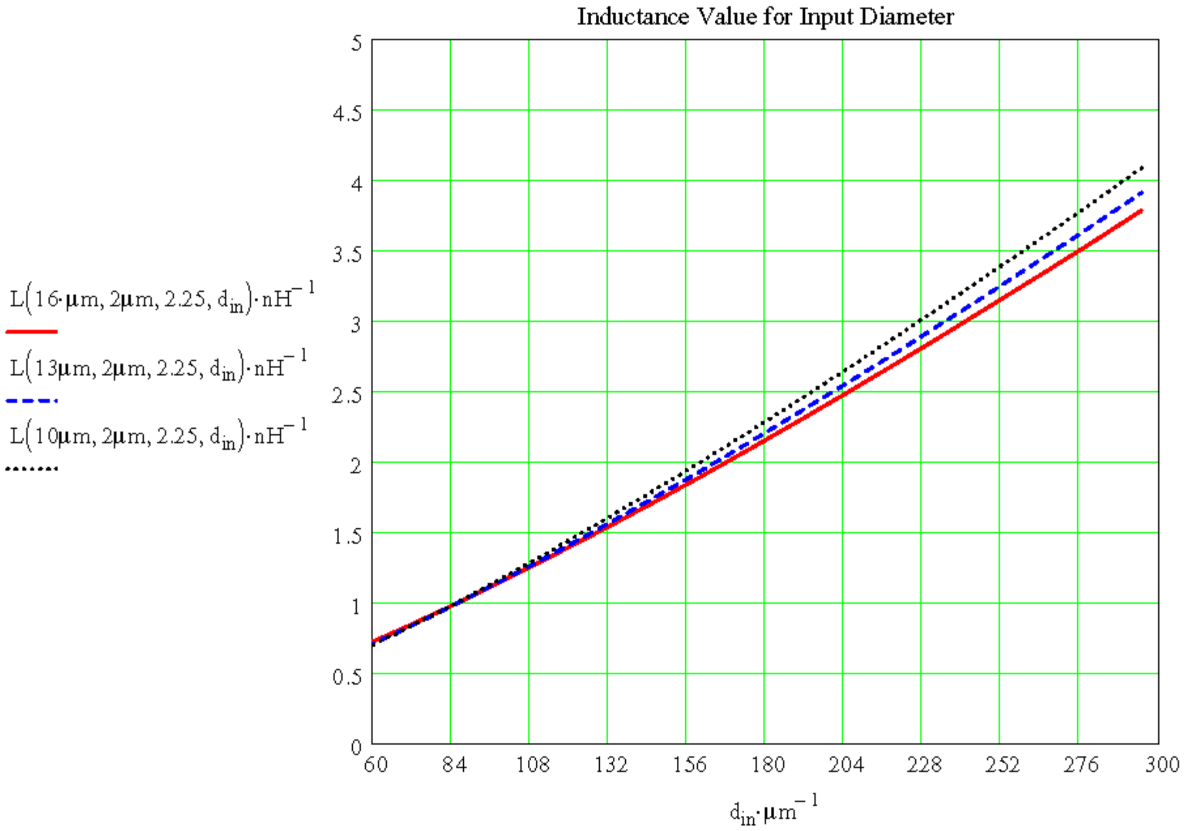
$d_{out}(w,s,n,d_{in}) := d_{in} + 2w + n \cdot (w+s) + (n-1)(w+s)$

$$\rho(w,s,n,d_{in}) := \frac{d_{out}(w,s,n,d_{in}) - d_{in}}{d_{out}(w,s,n,d_{in}) + d_{in}} \qquad d_{avg}(w,s,n,d_{in}) := \frac{d_{in} + d_{out}(w,s,n,d_{in})}{2}$$

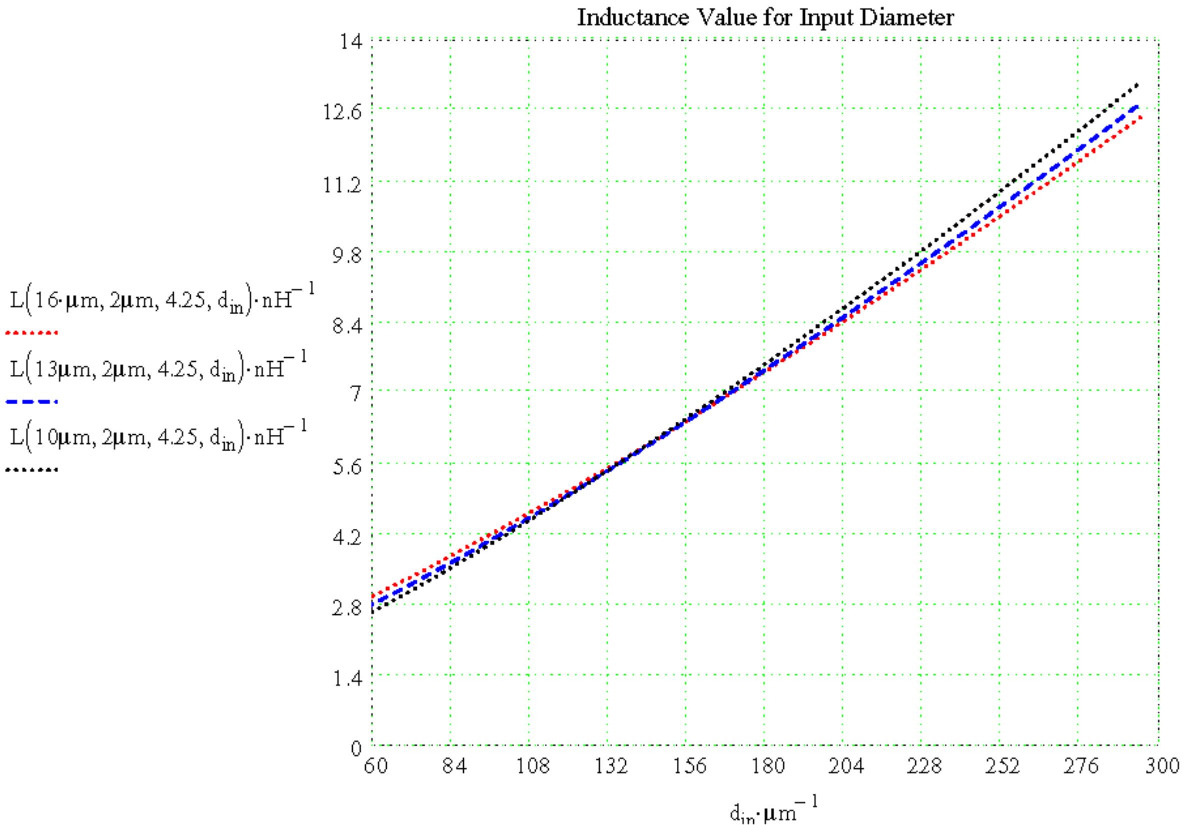
$$L(w,s,n,d_{in}) := \left[\frac{\mu_0 \cdot n^2 \cdot d_{avg}(w,s,n,d_{in}) \cdot C_{a1}}{2} \cdot \left(\ln\left(\frac{C_{a2}}{\rho(w,s,n,d_{in})}\right) + C_{a3} \cdot \rho(w,s,n,d_{in}) + C_{a4} \cdot \rho(w,s,n,d_{in})^2\right)\right]$$



$d_{out}(13\mu m, 2\mu m, 3.25, 125\mu m) = 233.5\mu m$



$d_{out}(13\mu m, 2\mu m, 2.25, 235\mu m) = 313.5\mu m$



$d_{out}(13\mu m, 2\mu m, 4.25, 85\mu m) = 223.5\mu m$

Transformer Directional Coupler

Chris Haji-Michael

This mathcad document is to design a directional coupler using transformers. The equations are from IEE Microwave Antennas and Prop, Vol 14, August 1999. The equations assume tight transformer coupling from 1 to N and are therefore this is only a starting point for a circuit built on a chip.

$$d(N_1,N_2) := 4\cdot N_1^{\,2}\cdot N_2^{\,2} + 1 + (N_1 - N_2)^2$$

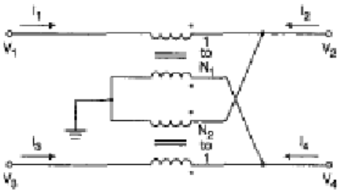


Fig.1 *Directional coupler with transformers*

$$S_{11}(N_1,N_2) := \frac{1}{d(N_1,N_2)}\left(-N_1^{\,2} + N_2^{\,2} - 2\cdot N_1\cdot N_2 + 1\right)$$

$$S_{22}(N_1,N_2) := \frac{1}{d(N_1,N_2)}\left(-N_1^{\,2} + N_2^{\,2} + 2\cdot N_1\cdot N_2 - 1\right)$$

$$S_{21}(N_1,N_2) := 20\cdot\log\left[\frac{2\cdot N_1\cdot N_2}{d(N_1,N_2)}(2\cdot N_1\cdot N_2 - 1)\right]$$

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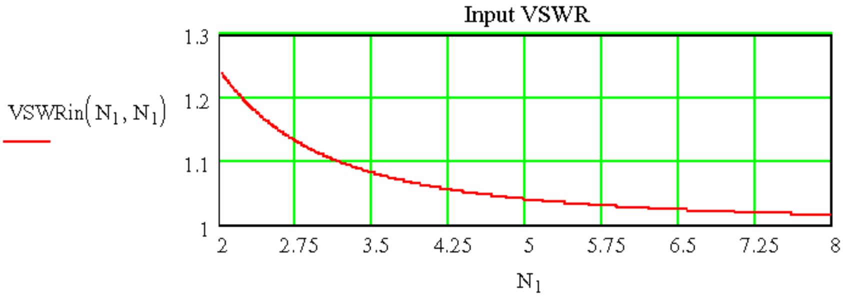
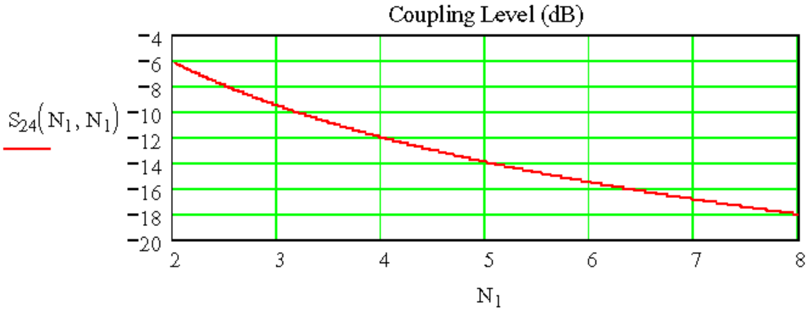
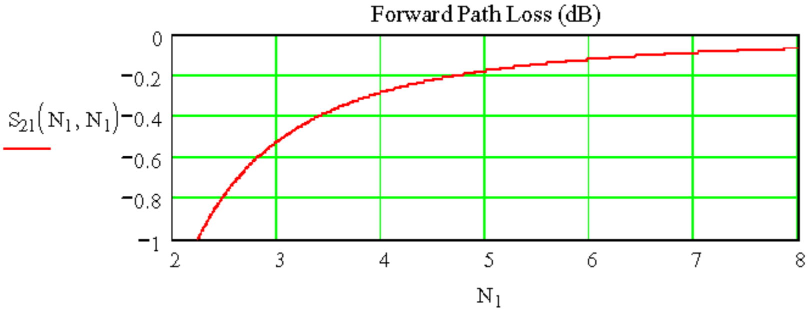
$$S_{24}(N_1,N_2) := 20\cdot\log\left[\frac{2\cdot N_1\cdot N_2}{d(N_1,N_2)}(N_1 + N_2)\right]$$

$$\mathrm{VSWRin}(N_1,N_2) := \frac{1 + |S_{11}(N_1,N_2)|}{1 - |S_{11}(N_1,N_2)|}$$



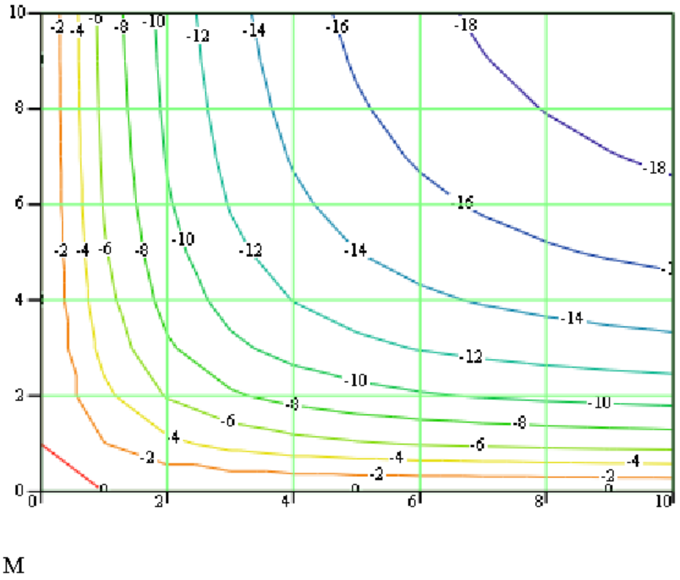




$N1 := 1, 2 .. 10 \qquad N2 := 1, 2 .. 10$

$M_{N1,N2} := S_{24}(N1, N2)$

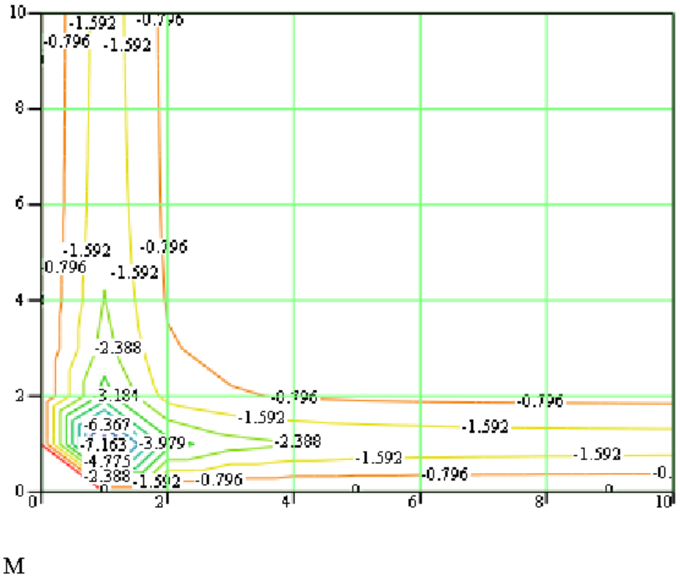
S24 (Return Coupling) in dB for N1 and N2



According to the paper the forward and reverse path losses, S21, S12, S34, S43 are all equal and calculated above as S21. Shown below dB. Added coil losses make a big difference to this.

$M_{N1,N2} := S_{21}(N1, N2)$

S21 (Ideal Forward Path Loss) in dB for N1 and N2

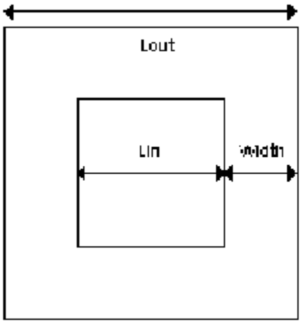


Transformer Capacitance Calculator

Chris Haji-Michael

This sheet is used to calculate the inter-winding capacitance for the transformer coupler using the simple capacitance equation. The width (W) & spacing (S) of the bottom winding reduces the capacitance compared to a flat plate. The top two turns are assumed to be a flat plate.

$\varepsilon_o := 8.854187817 \cdot 10^{-12} \cdot \frac{\text{farad}}{\text{m}}$ $\quad \varepsilon_r := 4.1 \quad \text{pF} := 10^{-12}\text{F} \quad \mu\text{m} := 10^{-6}\text{m}$



$$W_{eff}(W,T,H) := \begin{cases} W + 1.25 \cdot \left(\frac{T}{\pi}\right)\left(1 + \ln\left(\frac{4\cdot\pi\cdot W}{T}\right)\right) & \text{if } \frac{W}{H} < \frac{1}{2\cdot\pi} \\ W + 1.25 \cdot \left(\frac{T}{\pi}\right)\left(1 + \ln\left(\frac{4\cdot\pi\cdot W}{T}\right)\right) & \text{if } \frac{W}{H} = \frac{1}{2\cdot\pi} \\ W + 1.25 \cdot \left(\frac{T}{\pi}\right)\left(1 + \ln\left(\frac{2\cdot H}{T}\right)\right) & \text{if } \frac{W}{H} > \frac{1}{2\cdot\pi} \end{cases}$$

$W_{eff}(8\mu\text{m}, 0.6\mu\text{m}, 1\mu\text{m}) = 8.526\,\mu\text{m}$

$\text{Lin}(\text{Lout}, \text{Width}) := \text{Lout} - 2\cdot\text{Width} \qquad \text{Lin}(260\mu\text{m}, 80\mu\text{m}) = 100\,\mu\text{m}$

$$C(\text{Lout}, \text{Width}, \text{Depth}) := \frac{\text{Lout}^2 \cdot \varepsilon_r \cdot \varepsilon_o}{\text{Depth}} - \frac{\text{Lin}(\text{Lout}, \text{Width})^2 \cdot \varepsilon_r \cdot \varepsilon_o}{\text{Depth}}$$

Simple Capacitance equation

$$\text{Cap}(\text{Lout}, \text{Width}, \text{Depth}, W, S, T) := \frac{C(\text{Lout}, \text{Width}, \text{Depth})}{\left(\frac{W_{eff}(W, T, \text{Depth}) + S}{W_{eff}(W, T, \text{Depth})}\right)}$$

The adjustment for the metal thickness is from I.J.Bahl, "Transmission Lines in Handbook of Microwave & Optical Components", Editor K Chang, Wiley 1989

$\text{Cap}(265\mu\text{m}, 80\mu\text{m}, 1\mu\text{m}, 8\mu\text{m}, 3\mu\text{m}, 0.6\mu\text{m}) = 1.59\,\text{pF}$

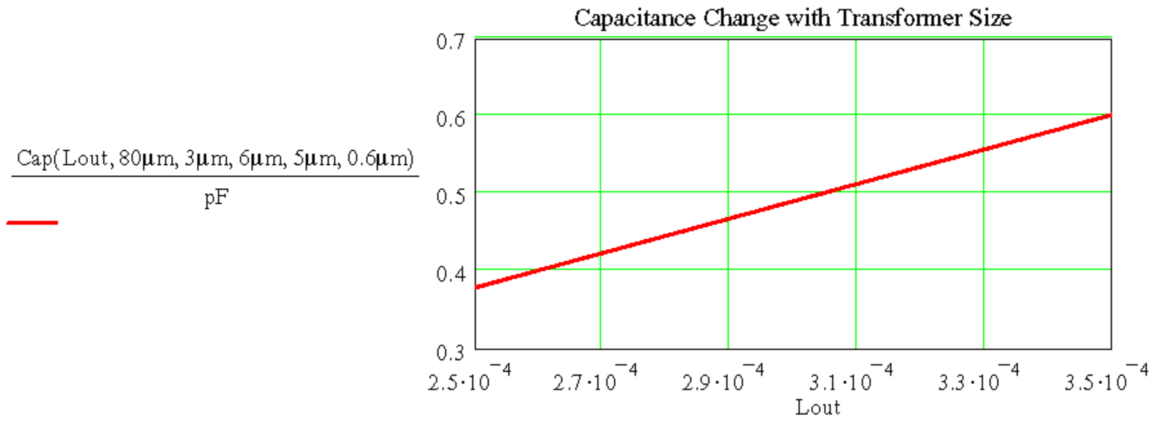
This is the interwinding capacitance for the original transformer, measured to be 1.6pF.

$\text{Cap}(265\mu\text{m}, 80\mu\text{m}, 3\mu\text{m}, 8\mu\text{m}, 3\mu\text{m}, 0.6\mu\text{m}) = 0.534\,\text{pF}$

This is the interwinding capacitance for the original transformer but with the windings placed on the Metal-2 Layer 3um from from M5.

$\text{Cap}(265\mu\text{m}, 80\mu\text{m}, 3\mu\text{m}, 6\mu\text{m}, 5\mu\text{m}, 0.6\mu\text{m}) = 0.413\,\text{pF}$

This is the interwinding capacitance when the secondary winding tracking is thinned to 6um with 5um spacing and on Metal-2.



APPENDIX B TEST SYSTEM

In order to test the IC in a repeatable and timely manner, two types of DC coupling boards were built to allow the voltages on the IC to be accurately set and a number of LabVIEW scripts were written.

The DC coupling boards are shown in Figures-B1 and B2. The input connection from the PSU is filtered using a low value resistor and a variety of capacitors. Both boards are similar but differ in the way the sense connection is made back to the PSU. The board in Figure B1 has the sense connection taken from the board, whereas the DC coupling board shown in Figure B2 uses a differential probe to take the sense connection directly from the amplifier or gain-block on the IC.

The method of taking the sense connection back from the IC is to minimize the affect of the series dc connection resistance on the test results, which can be up to a 5-Ohm. In addition, simulations of amplifier stability have shown that a 10-Ohm series resistor is required to ensure that the amplifier remains stable with an inductive power connection and this is fitted as part of the decoupling board. As the current through this path is expected to be 15mA, the combined resistance could result in a 225mV voltage drop. Taking the sense connections back from the IC ensures this voltage on the IC is accurately set. The board also provides generous power supply filtering capacitors.

The LabView virtual instruments (vi) and their function are listed here.

Page	Description	File Name
99	This vi plots the change in drain current on TR1 with the change in gate voltage. The results are stored in a file. This vi allows the bias point of TR1 to be set.	Plot_Id-Vg.vi
	This vi is similar to the previous, but changes the source voltage to the output transistor TR2.	Plot_Id-Vs.vi
99	This vi is used to set the dc conditions of the amplifier and gain-block before other tests are made. The dc conditions are automatically set when the “Automatic Tune up” button is pressed. This vi also measures and displays the input resistance and the currents.	DC_tune.vi
100	This vi plots the Log-Mag S21 & S12 directly from the Network Analyzer.	Log-Mag_S21_S12.vi
	This is a copy of the standard university vi script for capturing 2-port S parameters, but with project specific settings to reduce the chance of errors.	2 Port Single Shot Measurement.vi
100	This measures the NF from 1 to 2.5GHz. It sets the NF meter into mode-5 and loads up the ENR table. It is essential to use an LNA for accurate measurements. This script calibrates the measurement first.	Noise_figure.vi
101	This VI measures the IIP3 point from 1GHz to 2.5GHz. The signal generator power levels into the amplifier need to be accurately before testing. The outputs from both signal generators are combined as shown in Figure-B8.	IIP3.vi

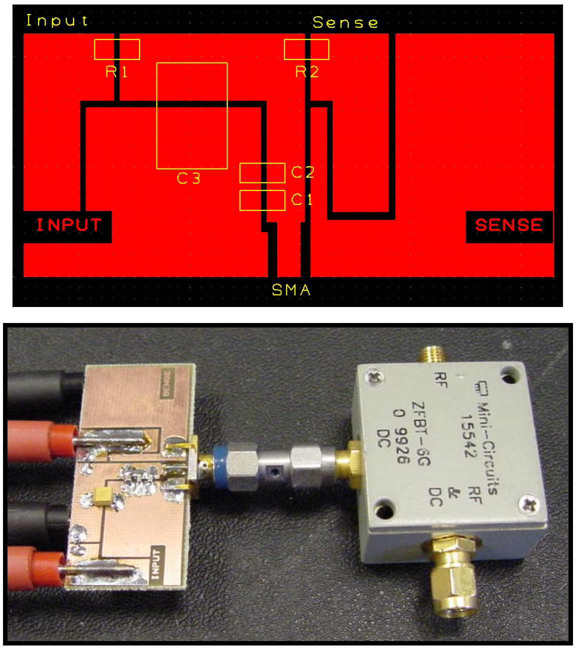

Input
Sense
R1
R2
C3
C2
C1
INPUT
SENSE
SMA
Mini-Circuits
15542
ZFBT-6G
0 9926
RF
RF & DC
DC

Figure B1 – DC Bias Board for putting DC on the Gate and Source of the Amplifier through a bias-T. The sense connection is made on the board. Two of these boards are required.

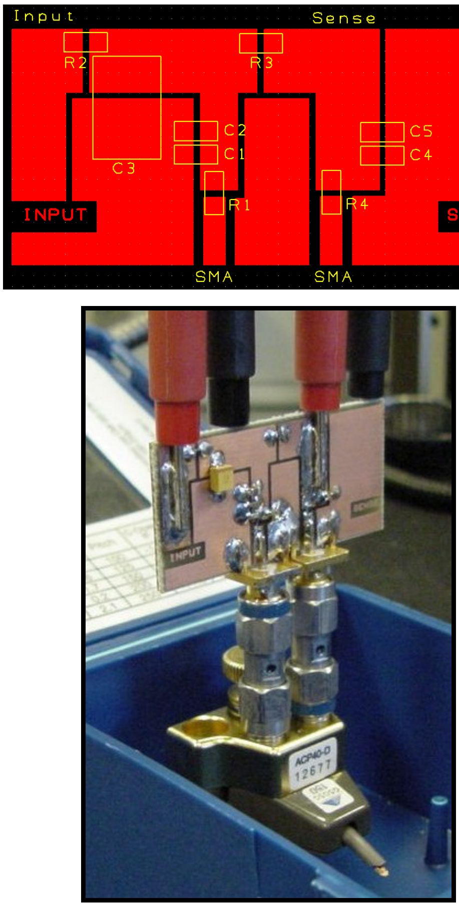
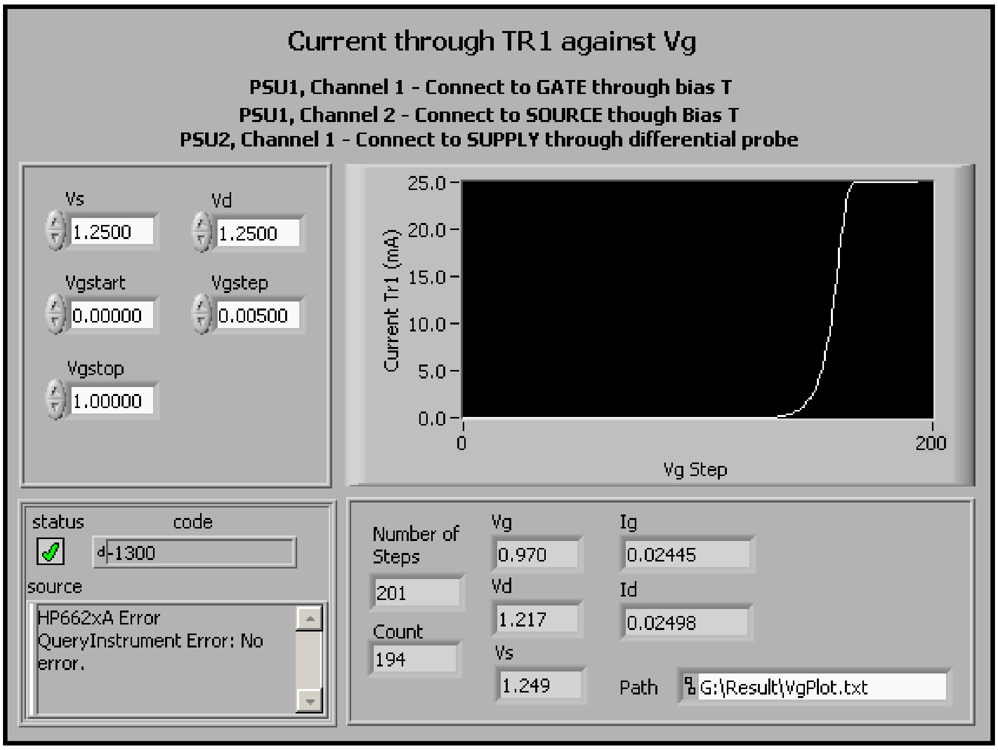

Input
Sense
R2
R3
C2
C1
C3
C5
C4
R1
R4
INPUT
SENSE
SMA
SMA
ACP40-D
12677

Figure B2 – DC Bias Board to put DC power on the Drain of the Amplifier. This connects to a differential probe so that the sense connection is taken directly from the IC.



Current through TR1 against Vg

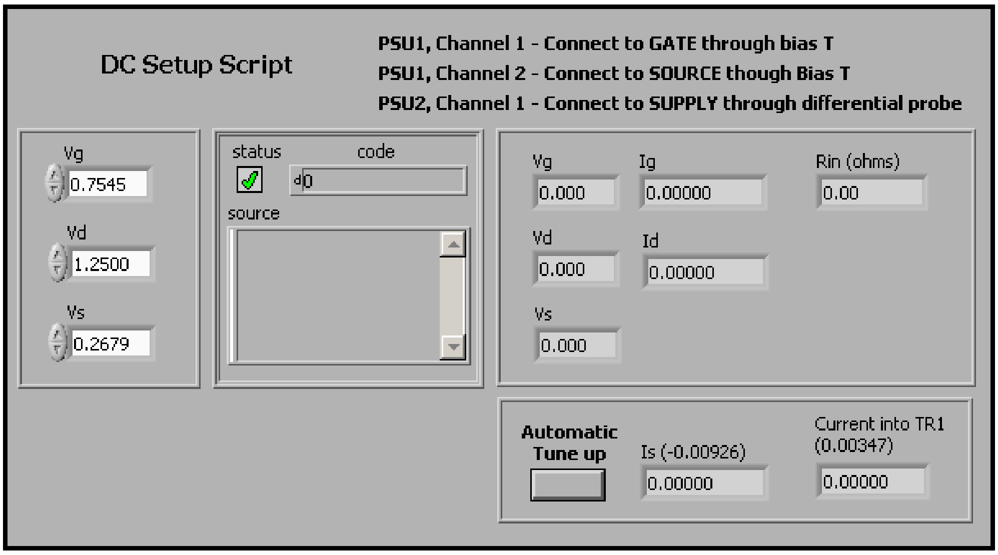
PSU1, Channel 1 - Connect to GATE through bias T
PSU1, Channel 2 - Connect to SOURCE though Bias T
PSU2, Channel 1 - Connect to SUPPLY through differential probe

Vs: 1.2500
Vd: 1.2500
Vgstart: 0.00000
Vgstep: 0.00500
Vgstop: 1.00000

status: ☑
code: -1300
source: HP662xA Error QueryInstrument Error: No error.

Number of Steps: 201
Count: 194
Vg: 0.970
Vd: 1.217
Vs: 1.249
Ig: 0.02445
Id: 0.02498
Path: G:\Result\VgPlot.txt

Figure B3 - LabView VI for measuring Vg-Id curve for FET



DC Setup Script

PSU1, Channel 1 - Connect to GATE through bias T
PSU1, Channel 2 - Connect to SOURCE though Bias T
PSU2, Channel 1 - Connect to SUPPLY through differential probe

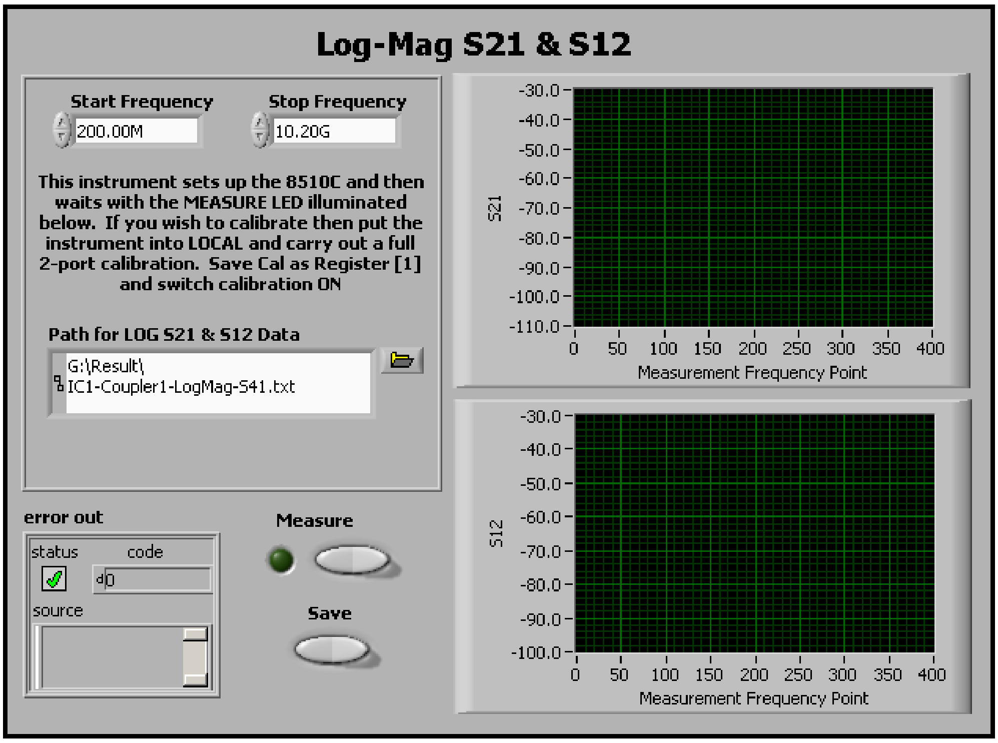
Vg: 0.7545
Vd: 1.2500
Vs: 0.2679

status: ☑
code: 0
source:

Vg: 0.000
Vd: 0.000
Vs: 0.000
Ig: 0.00000
Id: 0.00000
Rin (ohms): 0.00

Is (-0.00926): 0.00000
Current into TR1 (0.00347): 0.00000

Figure B4 - LabView VI for setting the Amplifier Operating Point



Log-Mag S21 & S12

Start Frequency: 200.00M

Stop Frequency: 10.20G

This instrument sets up the 8510C and then waits with the MEASURE LED illuminated below. If you wish to calibrate then put the instrument into LOCAL and carry out a full 2-port calibration. Save Cal as Register [1] and switch calibration ON

Path for LOG S21 & S12 Data: G:\Result\IC1-Coupler1-LogMag-S41.txt

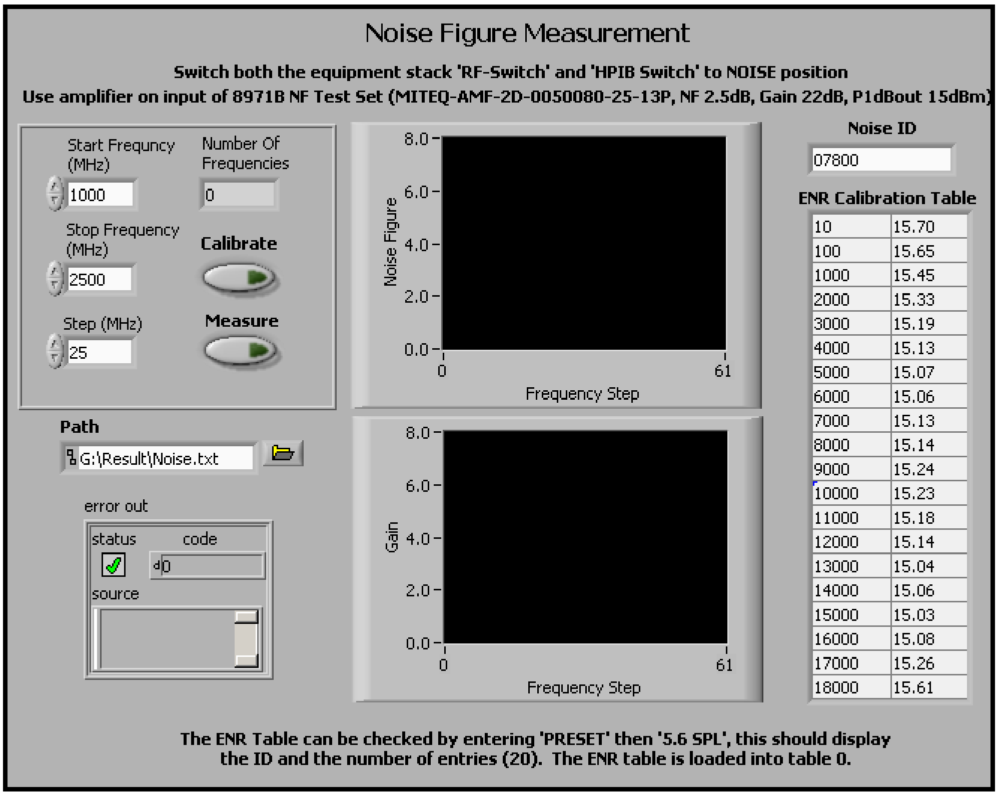
error out

status ☑ code 0

source

Measure
Save
S21
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
-110.0
0
50
100
150
200
250
300
350
400
Measurement Frequency Point
S12
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
0
50
100
150
200
250
300
350
400
Measurement Frequency Point

Figure B5 - LabView VI for measuring the Log-Mag S21 and S12



Noise Figure Measurement

Switch both the equipment stack 'RF-Switch' and 'HPIB Switch' to NOISE position
Use amplifier on input of 8971B NF Test Set (MITEQ-AMF-2D-0050080-25-13P, NF 2.5dB, Gain 22dB, P1dBout 15dBm)

Start Frequncy (MHz): 1000

Number Of Frequencies: 0

Stop Frequency (MHz): 2500

Step (MHz): 25

Path: G:\Result\Noise.txt

error out

status ☑ code 0

source

Noise ID: 07800

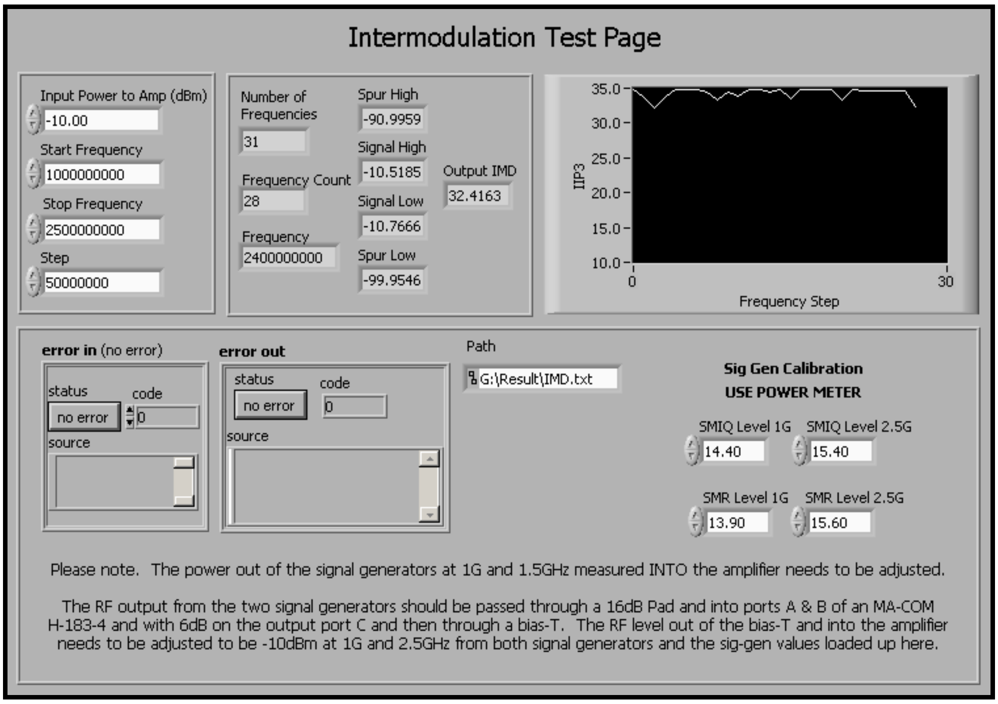
ENR Calibration Table

10	15.70
100	15.65
1000	15.45
2000	15.33
3000	15.19
4000	15.13
5000	15.07
6000	15.06
7000	15.13
8000	15.14
9000	15.24
10000	15.23
11000	15.18
12000	15.14
13000	15.04
14000	15.06
15000	15.03
16000	15.08
17000	15.26
18000	15.61

The ENR Table can be checked by entering 'PRESET' then '5.6 SPL', this should display the ID and the number of entries (20). The ENR table is loaded into table 0.

Calibrate
Measure
Noise Figure
8.0
6.0
4.0
2.0
0.0
0
61
Frequency Step
Gain
8.0
6.0
4.0
2.0
0.0
0
61
Frequency Step

Figure B6 - LabView VI for measuring the NF from 1GHz to 2.5GHz



Intermodulation Test Page

Input Power to Amp (dBm) -10.00
Start Frequency 1000000000
Stop Frequency 2500000000
Step 50000000

Number of Frequencies 31
Frequency Count 28
Frequency 2400000000

Spur High -90.9959
Signal High -10.5185
Signal Low -10.7666
Spur Low -99.9546
Output IMD 32.4163

error in (no error)
status no error
code 0
source

error out
status no error
code 0
source

Path G:\Result\IMD.txt

Sig Gen Calibration
USE POWER METER
SMIQ Level 1G 14.40
SMIQ Level 2.5G 15.40
SMR Level 1G 13.90
SMR Level 2.5G 15.60

Please note. The power out of the signal generators at 1G and 1.5GHz measured INTO the amplifier needs to be adjusted.

The RF output from the two signal generators should be passed through a 16dB Pad and into ports A & B of an MA-COM H-183-4 and with 6dB on the output port C and then through a bias-T. The RF level out of the bias-T and into the amplifier needs to be adjusted to be -10dBm at 1G and 2.5GHz from both signal generators and the sig-gen values loaded up here.

Figure B7 - LabView VI for measuring the Input Third Order Intermodulation Point from 1GHz to 2.5GHz

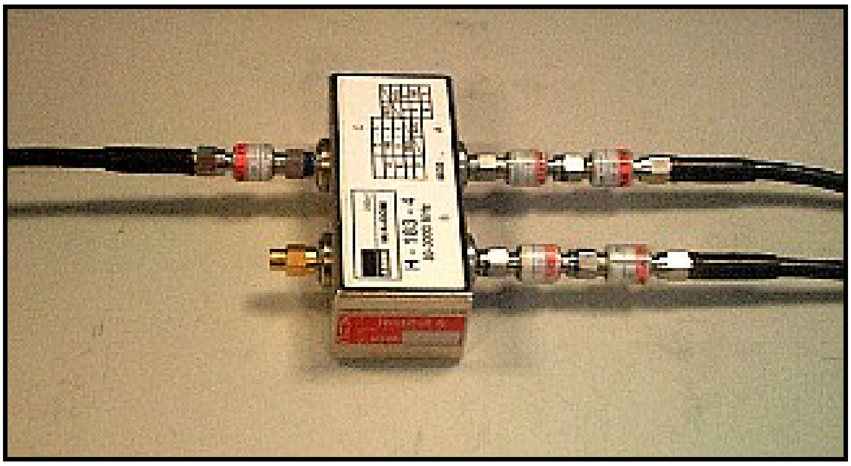


Figure B8 – Connection to the RF Coupler as required for the Intermodulation Test

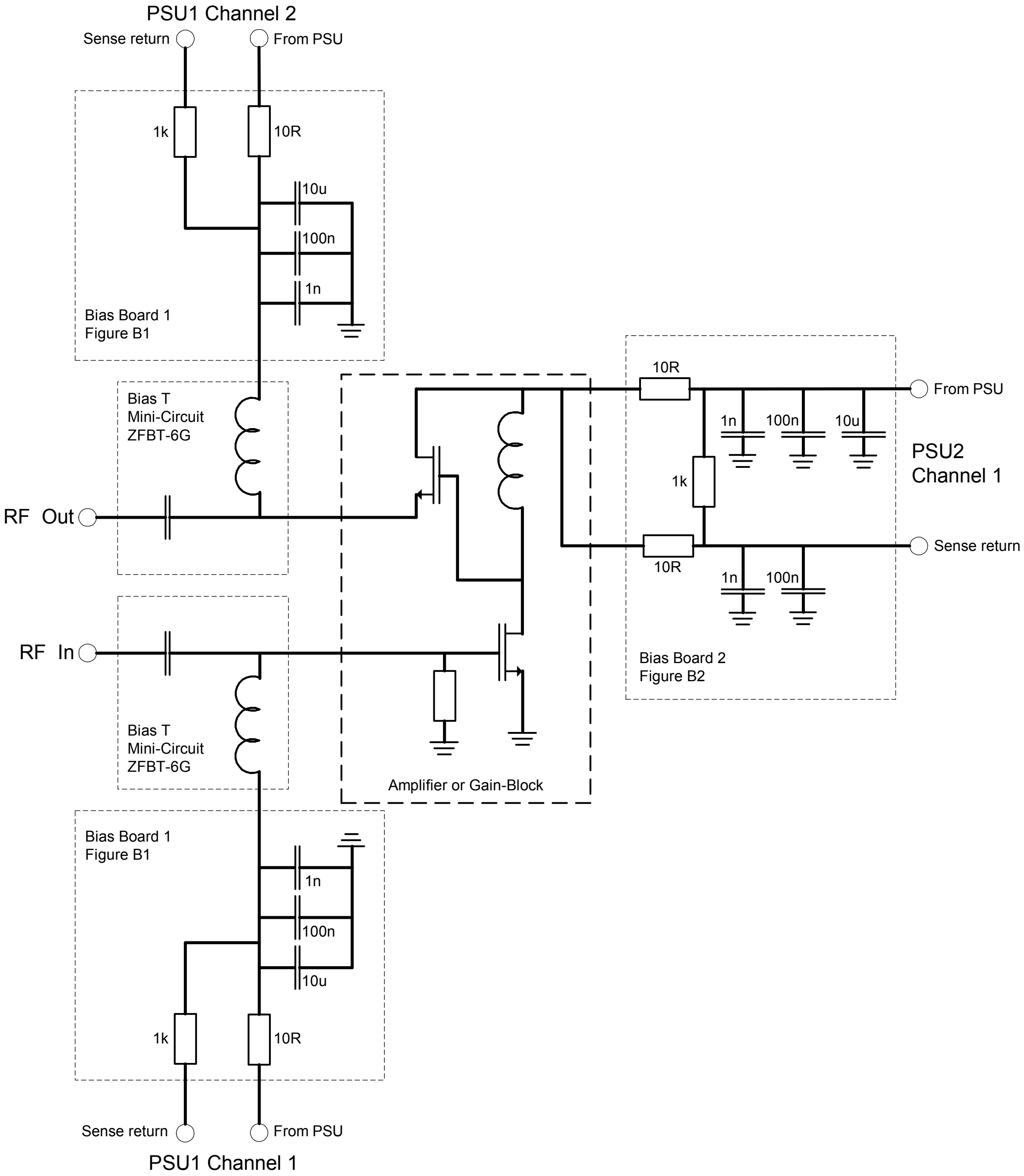

PSU1 Channel 2
Sense return
From PSU
1k
10R
10u
100n
1n
Bias Board 1
Figure B1
Bias T
Mini-Circuit
ZFBT-6G
RF Out
RF In
Amplifier or Gain-Block
10R
From PSU
1n
100n
10u
PSU2
Channel 1
1k
Sense return
10R
1n
100n
Bias Board 2
Figure B2
Bias T
Mini-Circuit
ZFBT-6G
Bias Board 1
Figure B1
1n
100n
10u
1k
10R
Sense return
From PSU
PSU1 Channel 1

Figure B9 – Power Connections to Amplifier Circuits. The schematics for both bias boards are shows here

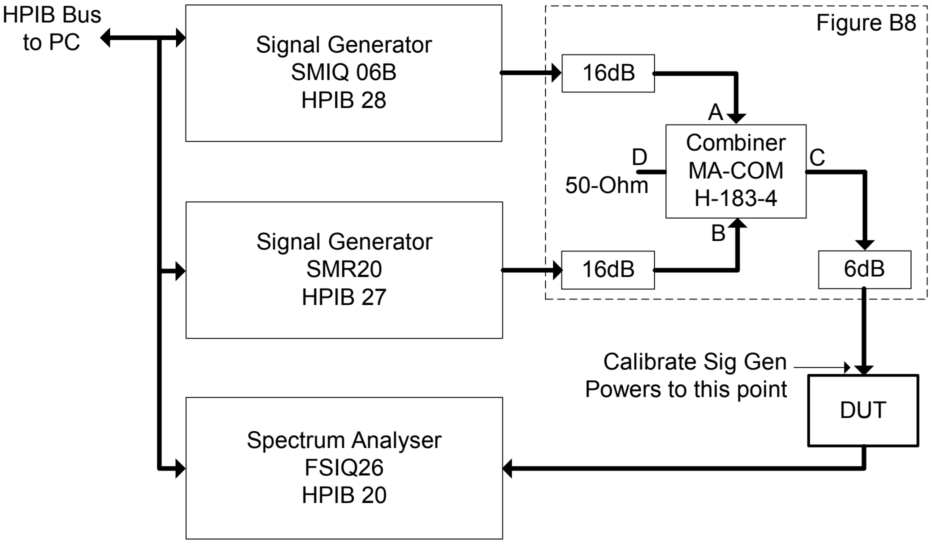

HPIB Bus
to PC
Signal Generator
SMIQ 06B
HPIB 28
Signal Generator
SMR20
HPIB 27
Spectrum Analyser
FSIQ26
HPIB 20
Figure B8
16dB
16dB
A
B
C
D
50-Ohm
Combiner
MA-COM
H-183-4
6dB
Calibrate Sig Gen
Powers to this point
DUT

Figure B10 – Equipment Connection for the Intermodulation test.

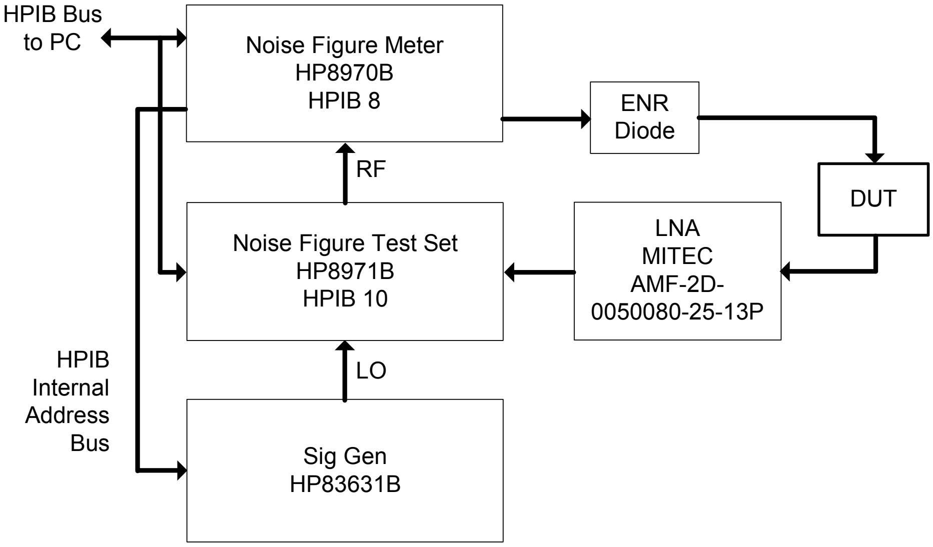
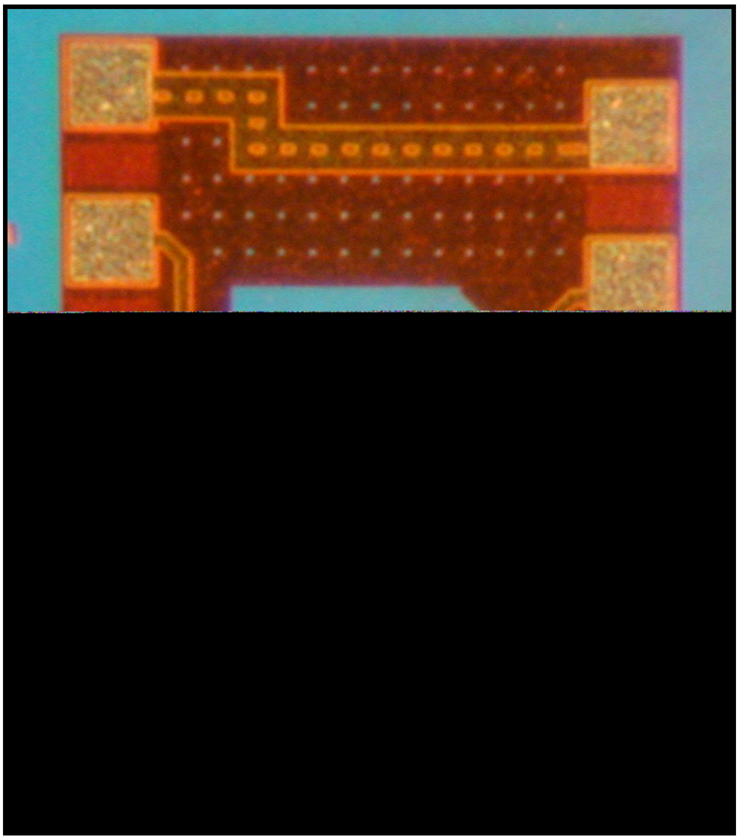
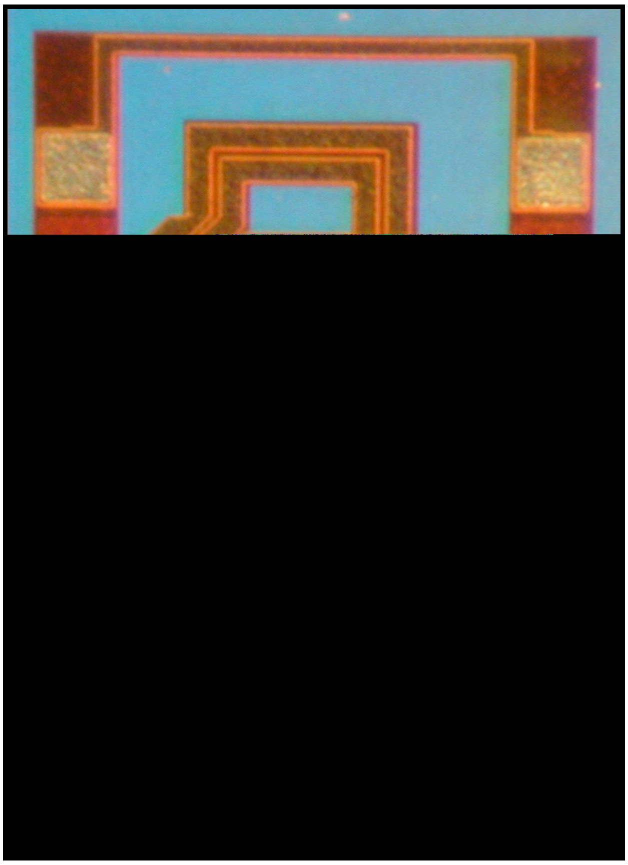

HPIB Bus
to PC
Noise Figure Meter
HP8970B
HPIB 8
ENR
Diode
DUT
RF
Noise Figure Test Set
HP8971B
HPIB 10
LNA
MITEC
AMF-2D-
0050080-25-13P
HPIB
Internal
Address
Bus
LO
Sig Gen
HP83631B

Figure B11 – Equipment Connection for the Noise Figure test.

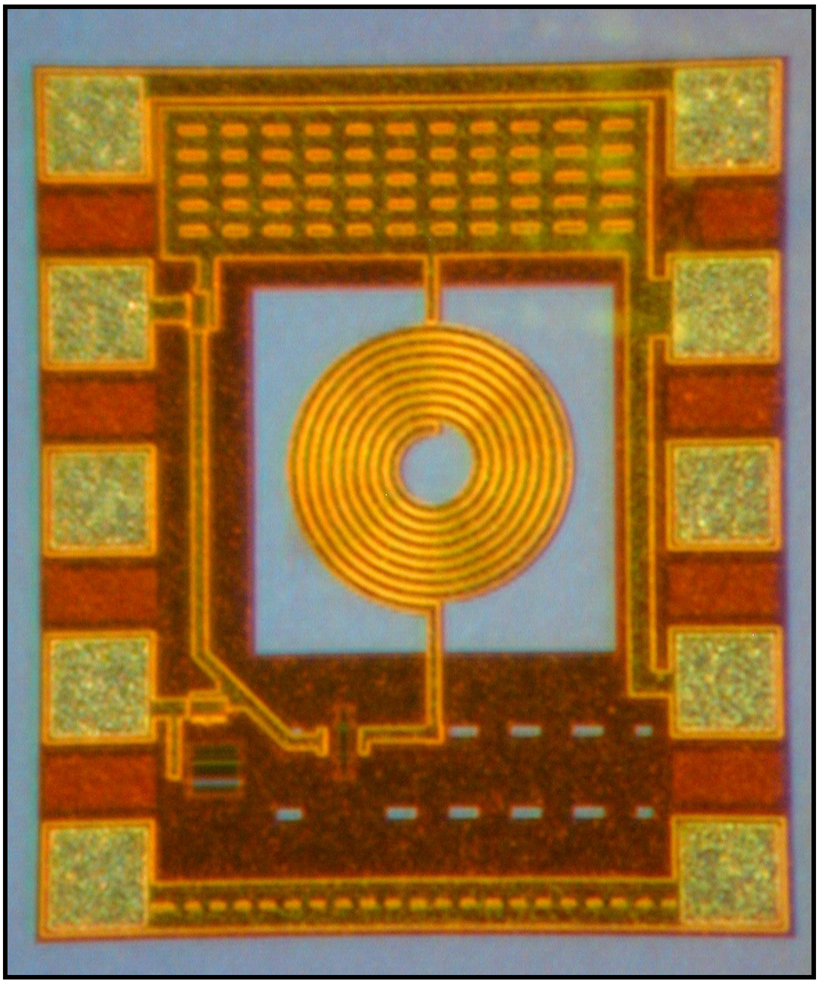
APPENDIX C PHOTOGRAPHIC IMAGES



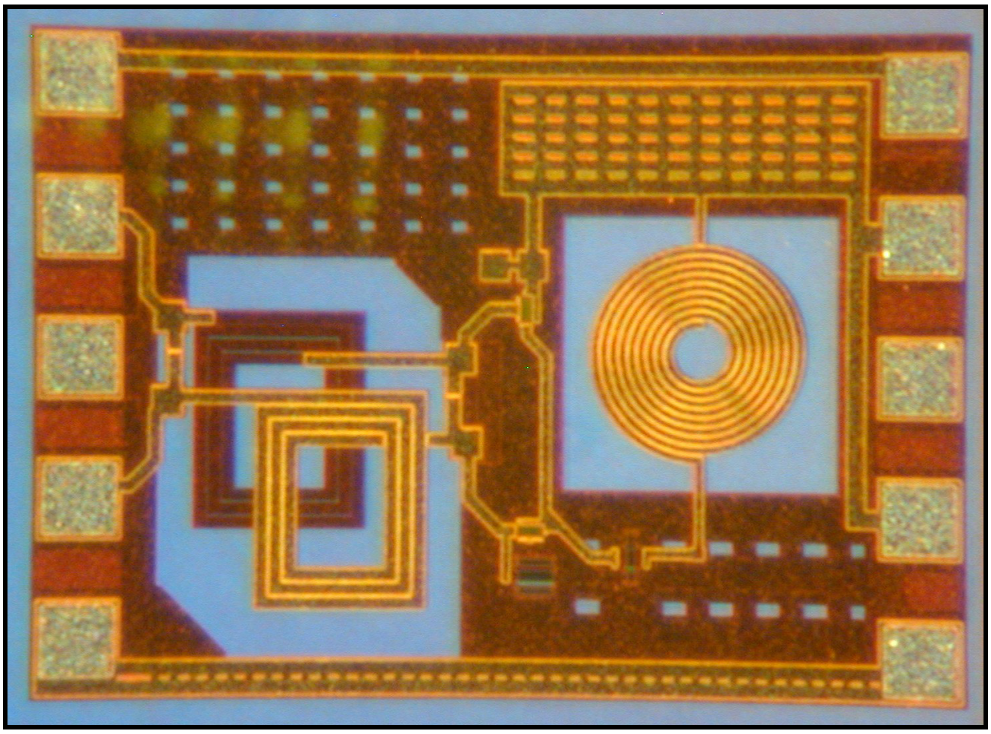
Lumped Element RF Directional Coupler



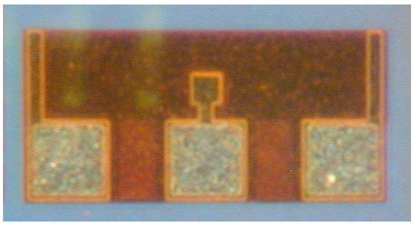
Transformer RF Directional Coupler



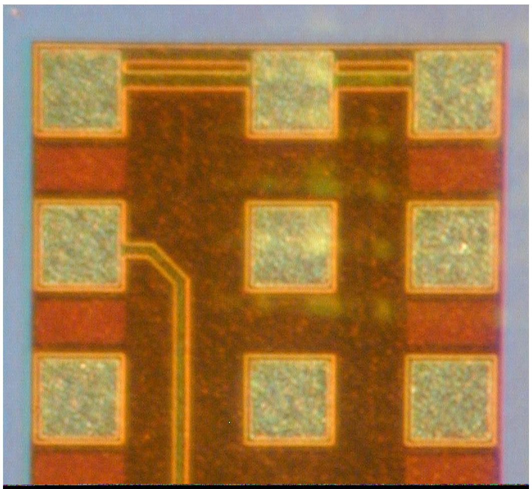
Gain Block



Lossless Feedback Amplifier



Test Structure to Measure 32um Capacitor



[redacted]

Calibration Structure to Calibrate through-path with differential Probe. Also contains Open and Short circuit pads.

APPENDIX D RESULTS DATA

The test data was imported into Excel spreadsheets for processing and plotting.

Description	File Name
Plots the Id against Vg for TR1 and calculates gm.	Id change with Vg, Vs=1.25.XLS
Analysis of the interwinding capacitance.	Coupler 2 Capacitor Analysis.xls
Analysis of the 32µm capacitor.	32um Capacitor Analysis.xls
Plots the S-parameters for the discrete component RF directional coupler and compares these with the simulated results.	IC1-Coupler1.xls
Plots the S-parameters for the Transformer RF directional coupler and compares these with the simulated results.	IC1-Coupler2.xls
Plots the IIP3 of both the amplifier & gain-block.	IC1-IMD.xls
Plots the Noise-Figure of both the amplifier & gain-block.	IC1-noise.xls
Plots the Gain of both the amplifier & gain-block.	IC1-gain.xls